

FabiaTech Corporation

IPC Solution

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ISA CPU Card

Low Power Series

FB2503 User's Manual

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If you have problems or difficulties in using the system board, or setting up the relevant devices, and software that are not explained in this manual, please contact our service engineer for service, or send email to support@fabiatech.com.

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If your board requires servicing, contact the dealer from whom you purchased the product for service information. You can help assure efficient servicing of your product by following these guidelines:

- ❑ A list of your name, address, telephone, facsimile number, or email address where you may be reached during the day
- ❑ Description of you peripheral attachments
- ❑ Description of you software (operating system, version, application software, etc.) and BIOS configuration
- ❑ Description of the symptoms (Extract wording any message)

For updated BIOS, drivers, manuals, or product information, please visit us at www.fabiatech.com

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Chapter 1 Introducing the FB2503 System Board

Overview

The FB2503 is a VIA Mark Low power processor, all in one, half-size ISA CPU card. This user's manual provides information on the physical features, installation, and BIOS setup of the FB2503.

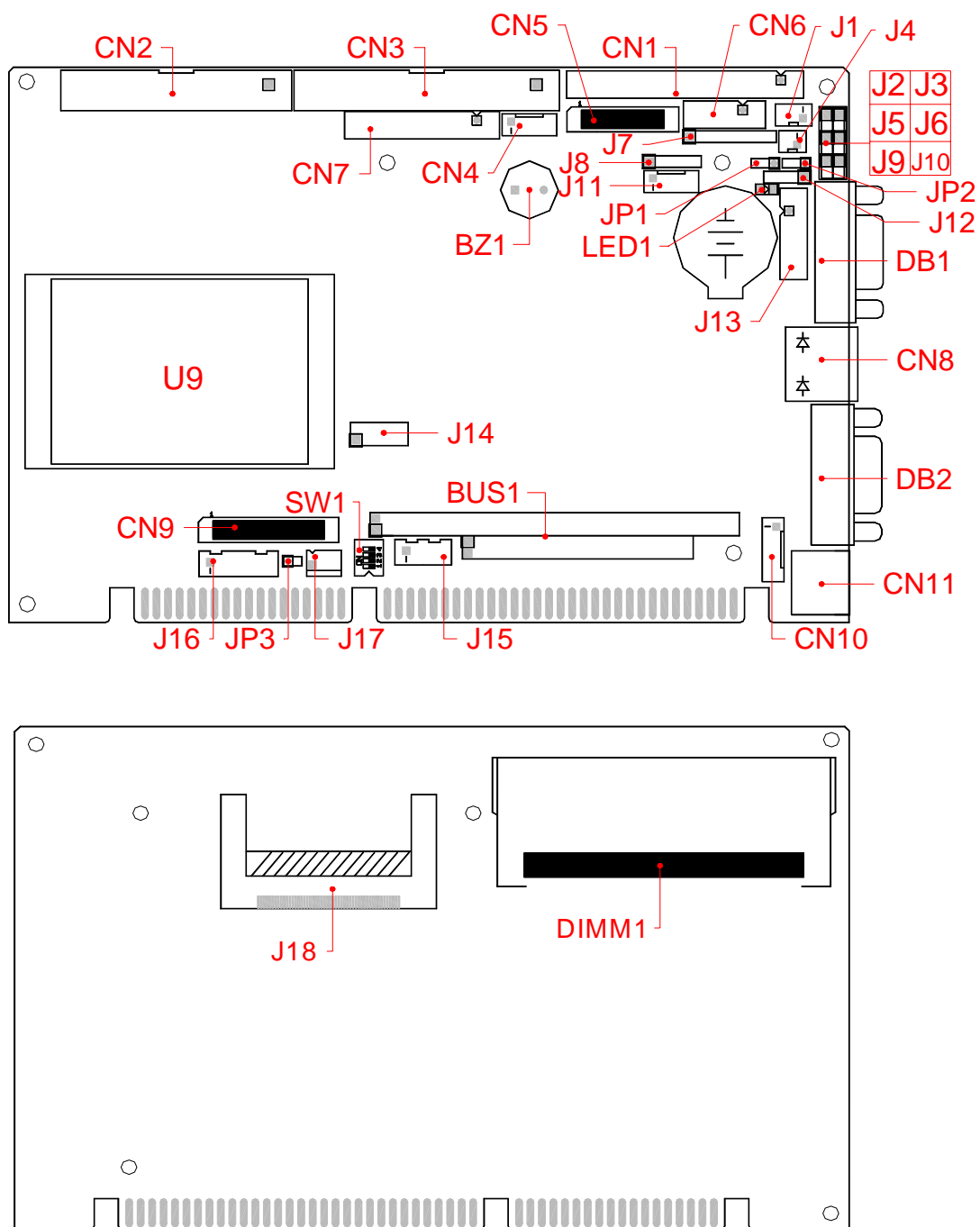
Built to unleash the total potential of the VIA Mark Core Fusion™ Processor, the FB2503 is a single boards computer capable of handling today's demanding requirements. Able to support 533Mhz ~800MHz CPUs, this unit supports 10/100M interface network port, synchronous pipeline burst SDRAM up to 578MB and a onboard VGA port up to 32MB share memory that can support TTL/LVDS LCD's and CRT's simultaneously or independently.

Each FB2503 has two ports for I/O communications. One RS-232C and one RS-232 /422/485 ports are available. There is also a watchdog timer that can be configured from software to automatically reset the system or generate an interrupt if there is a system's or EMI problem. And for easy configuration, AMI BIOS are available.

Power management is also featured to lower the rate of consumption. The unit supports doze mode, <Suspend Mode> and <Standby mode> as well as it adheres to the "Green Function" standard.

The FB2503 is perfect for POS and POI applications, network systems, panel / MMI's, order entry kiosks, test equipment, OEM projects or as a motherboard for a panel PC. The unit is only 185X122mm, offering unparalleled performance in a very small footprint.

Layout



Specifications

- Onboard 533Mhz VIA Mark Core Fusion™ Low Power CPU.
- VIA Mark Core Fusion™+VT82C686B chipset.
- Compact size slot card with ISA expansion bus.
- On-board 64MB SDRAM and 1 So-DIMM socket for up to 576MB maximum.
- 100M/10M Ethernet with RJ-45 connector.
- Onboard VGA port (VIA Mark Core Fusion™ Integrated ProSavage4 Graphic) supports CRT and LVDS with up to 32MB shared memory.
- Parallel port, floppy and support two Enhanced IDE channels.
- One RS-232 and One RS-232/RS-422/RS-485/IrDA.
- PS/2 compatible keyboard and mouse interface.
- Compact Flash socket for 3.3V Compact Flash and Micro Drives.
- On-board buzzer and LED indicator.
- Software programmable watchdog timer.
- Two USB ports and hardware monitoring functions.
- Provides two CPU & case cooling fan connector for monitoring.
- Provides One AC97 and One feature connector for Audio function. **(Optional)**.
- Flash BIOS with easy upgrade utility.
- Compact size, 185 mm x 122 mm.

Packing List

Upon receiving the package, verify the following things. Should any of the mentioned happens, contact us for immediate service.

- Unpack and inspect the FB2503 package for possible damage that may occur during the delivery process.
- Verify the accessories in the package according to the packing list and see if there is anything missing or incorrect package is included.
- If the cable(s) you use to install the FB2503 is not supplied from us, please make sure the specification of the cable(s) is compatible with the FB2503 system board.

Note: after you install the FB2503, it is recommended that you keep the diskette or CD that contains drivers and document files, document copies, and unused cables in the cartoon for future use.

The following lists the accessories that may be included in your FB2503 package. Some accessories are optional items that are only shipped upon order.

- One FB2503 system board
- One compact disc containing manual file in PDF format and necessary drivers and utilities
- One 40-pin hard disk drive interface cable
- One 34-pin floppy drive interface cable
- One serial port and parallel port interface cable with bracket
- One mouse port adapter cable with bracket
- One hard copy of Quick Installation Guide
- One 2-port USB adapter cable (**Optional**)

Chapter 2 Hardware Installation

To set up a FB2503 system board, complete the description Chapter 2 and Chapter 3.

This chapter introduces the system board connectors, jumper settings and then guides you to apply them for field application.

Before Installation

Before you install the system board, make sure you follow the following descriptions.

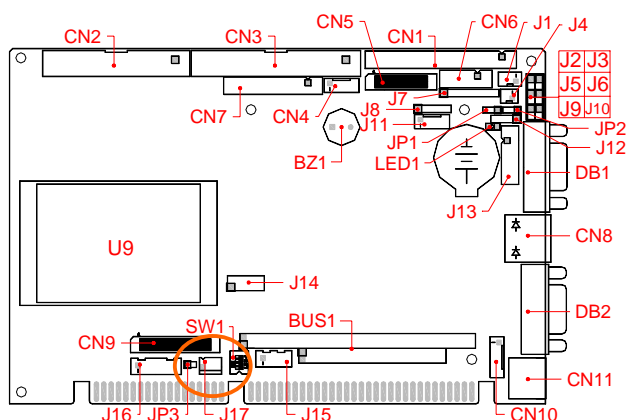
1. Before removing the board from its anti-static bag, wear an anti-static strap to prevent the generation of Electricity Static Discharge (ESD). The ESD may be created from human body that touches the board. It may do damage to the board circuit.
2. Install or unplug any connector, module, or add-on card, be sure that the power is disconnected from the system board. If not, this may damage the system board components, module, or the add-on-card.
3. Installing a heat sink and cooling fan is necessary for heat dissipation from your CPU. If heat sink or cooling fan is not mounted, this may cause the CPU fail due to over-heating problem.
4. When you connect the connectors and memory modules, be careful with the pin orientations.

Hardware Features

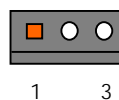
The following lists the connectors and jumpers to install the FB2503.

Item	Description
CN1	44-pin 2.0mm IDE 2 hard disk connector (IDC).
CN2	34-pin 2.54mm floppy connector (IDC).
CN3	40-pin 2.54mm IDE 1 hard disk connector (IDC).
CN4	For Inverter connector (JST)
CN5	LCD Connector with 36 bit LVD signals (DF13)
CN6	10-pin RS-232 port 2 connector (IDC)
CN7	26-pin 2.0mm parallel port connector (IDC)
CN8	RJ45-Lan connector
CN9	LCD Connector with 24 bit TTL signals (DF13)
CN10, CN11	Keyboard and Mouse connector
J1	3-pin touch screen header for serial port 2
J2	2-pin HDD LED Indicator header
J3	ATX soft power switch header
J4	2-pin External battery header
J5	2-pin Reset header
J6	2-pin for external temperature sensor header
J7	Reserved
J8	5-pin RS232C IrDA header for serial port 2
J9	2-pin for external TX-LED header with LAN
J10	2-pin Power and watchdog header of LED indicator
J11	5-pin for TTL I/O (JST)
BZ1, J12	Onboard Buzzer and external speaker header
J13	AMR connector for provides AC97 signals for Audio and Modem functions
J14	10-pin USB connector
J15	Control signal for ATX power supply only
J16	6-pin power connector (JST)
J17	3-pin for case/CPU cooling fan t
J18, JP1	Compact Flash Socket and Master/Slave Select
JP2	To clear CMOS data
JP3	ATX and Non-ATX Select
DB1	CRT connector
DB2	RS232 9-pin D – type male connector
LED1	Power and watchdog of LED indicator
SW1	To selects RS422/RS485 and Terminator for serial port 2 and Memory Bank Select
BUS1	PC104 BUS Connector
DIM1	SDRAM So-DIMM Socket

□ J17: CPU Fan Connector



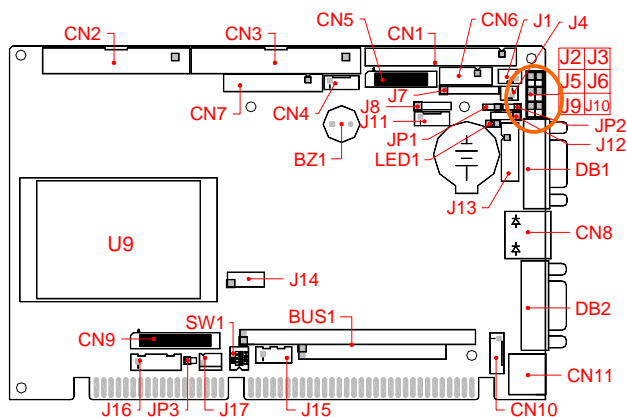
J17



J17	Description
1	Ground
2	+12V
3	Speed-In

□ J5: Reset Header

J5 is a 2-pin header for connecting to system reset bottom. Short-circuit these 2 pins to hardware reset FB2503 as well as restart system. It is similar to power off the system and then power it on again.

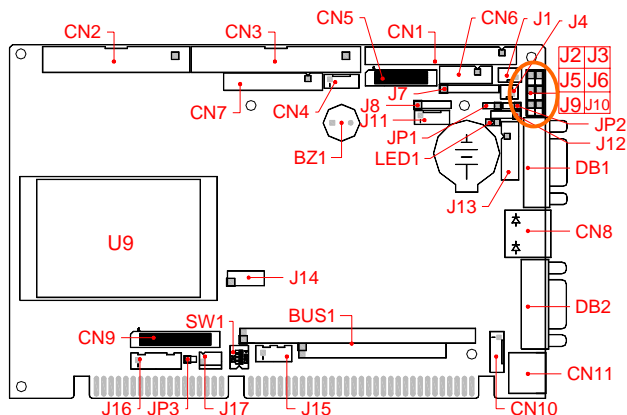


J5



Pin1 Reset +
Pin2 Reset -

□ J10: Power/Watchdog LED Header

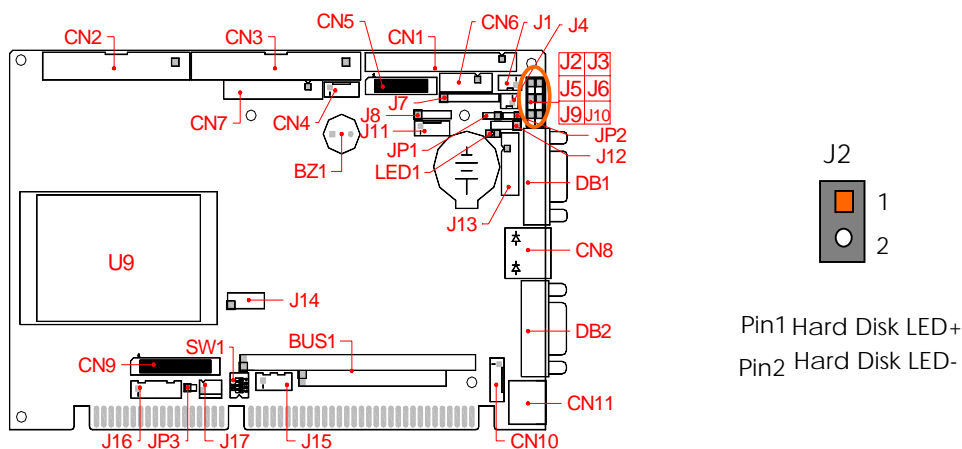


J10



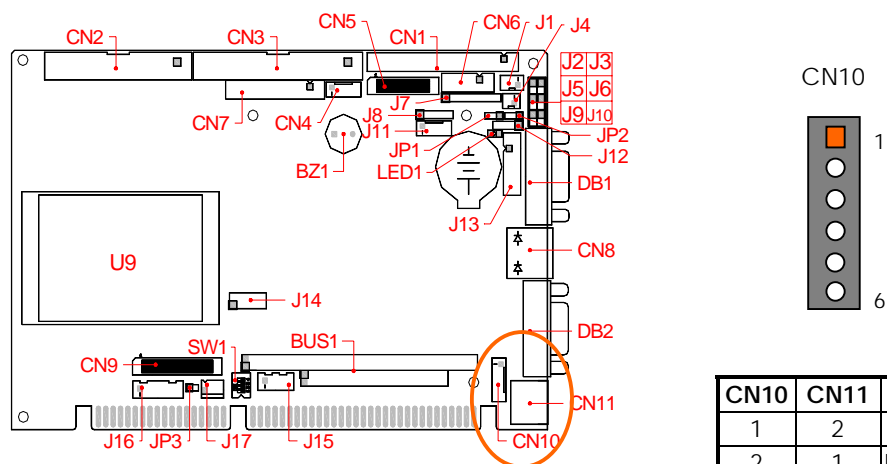
Pin 1 Power/Watchdog LED +
Pin 2 Power/Watchdog LED -

- **J2: HDD LED Header**

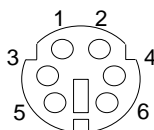


- **CN10, CN11: Keyboard/Mouse Connector**

CN11 is a standard PS/2 type keyboard connector, so any PS/2 type keyboard can plug into directly without extra adapter cable. CN10 provides PS/2 mouse interface, use the included mouse adapter cable to connect between CN10 and standard PS/2 mouse.



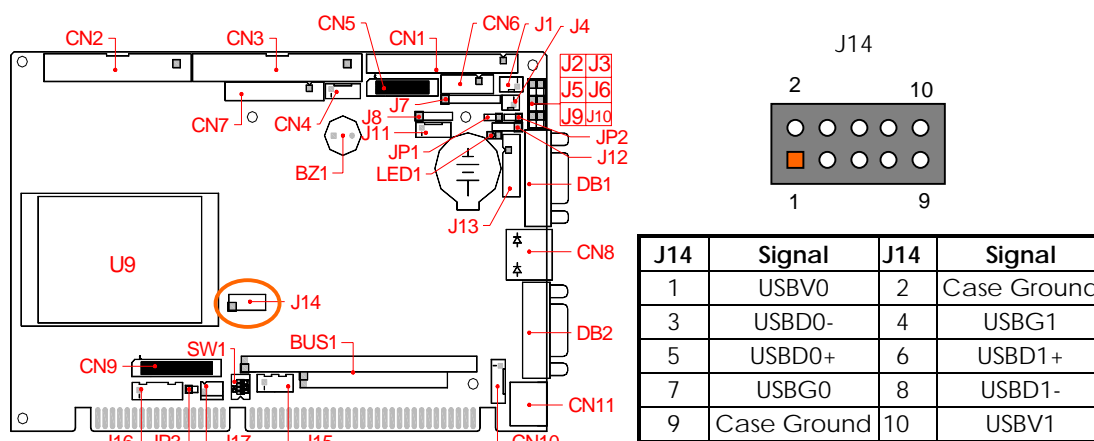
CN11 Front View



CN10	CN11	Signal
1	2	Mouse Data
2	1	Keyboard Data
3	3	Ground
4	4	VCC
5	6	Mouse Clock
6	5	Keyboard Clock

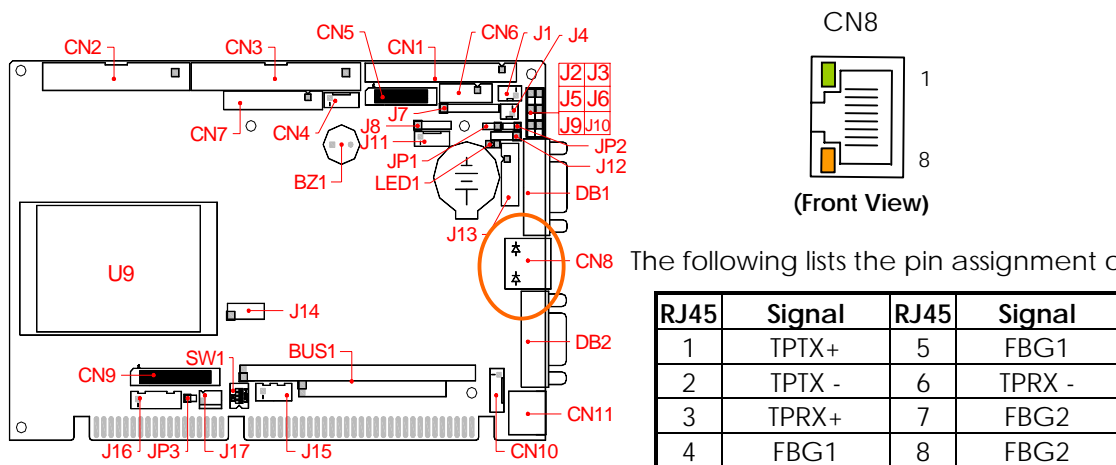
□ J14: USB Connector

J14 is a 10-pin connector. Use included adapter cable (Optional) for transferring to standard double port USB connector. The upper port is USB #0 and the lower port is USB#1



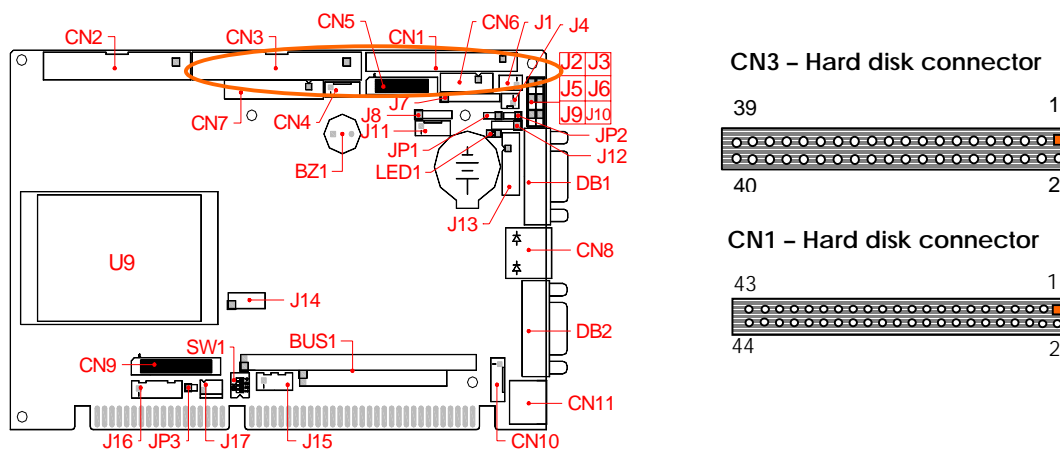
□ CN8: RJ45 LAN Connector

The CN8 contain LAN twist pair signals and LAN accesses indicator signal is RJ45 type connector with 2 LED indicators. The down side LED (orange) indicates data is accessing and the up side LED (green) indicates on-line status. (When lighted indicates on-line and off indicates off-line).



□ CN3, CN1: IDE hard Disk Connector

CN3 is 40-pin 2.54mm IDE hard disk connector. CN1 is 44-pin 2.0mm IDC connectors. The IDE interface has two enhanced IDE channels and supports 4 IDE devices with ultra DMA 33 and or IDE channel 1 IDE supports ultra DMA 33/66/100.



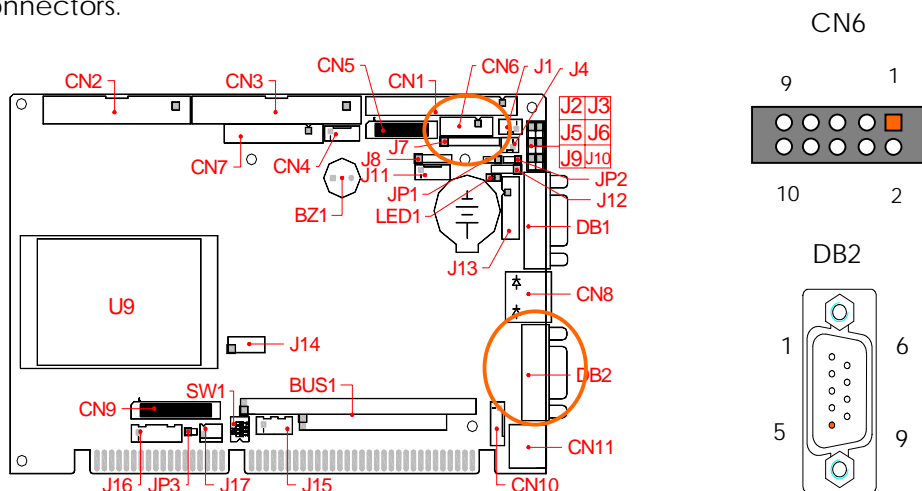
✧ Caution: If you use ULTRADMA/66/100 devices, you will need to purchase another UltraDMA/66/100 cable. UltraDMA/66/100 IDE devices must use a 40-pin 80-conductor IDE cable. (See P44 PERIPHERAL SET UP)

The following table lists the pin description of CN3, CN6.

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AINTE	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41 (CN1)	VCC	42 (CN1)	VCC
43 (CN1)	GROUND	44 (CN1)	Not Used

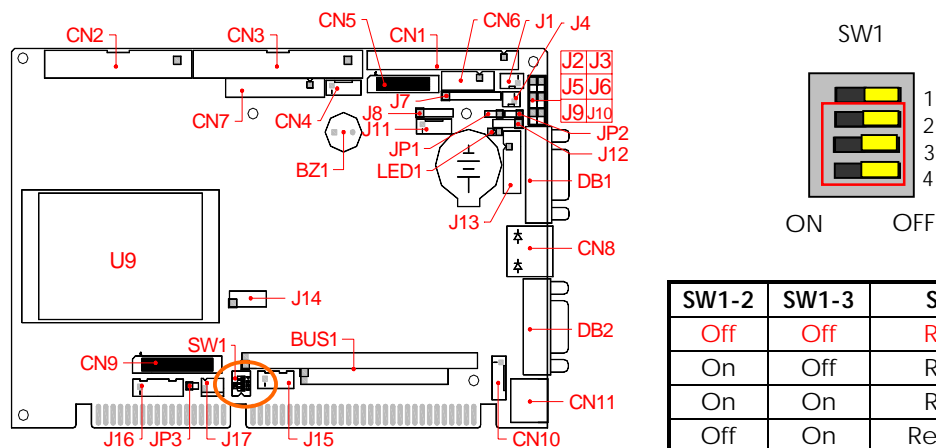
- DB2, CN6: RS232 Serial Ports 1,2 Connectors and Jumpers

The DB25 connector on bracket is 9-pin D-type male connector the serial port 25 pin adapter cables are used to transfer 25-pin IDC connector into standard DB25 connectors.



- ❑ **Serial Port 2 (CN6, SW1, J1, J8 and SW1)**

Serial port 2 is designed for multiple purposes. It could be RS-232C, RS-422 or RS-485 by selecting SW1 or changing the setting in BIOS setup program, and SW1-4 is used to enable or disable terminator if RS-485 mode is selected. Serial port 2 also could be configured as Infra (IrDA) interface by changing the setting in BIOS setup program. J8 is used to interface with Infra module. When touch screen module is used, you could connect J1 to touch screen controller directly and internally instead of connect from CN6 connector.



SW1-2	SW1-3	Signal
Off	Off	RS-232
On	Off	RS-422
On	On	RS-485
Off	On	Reserved

Factory Preset: RS232

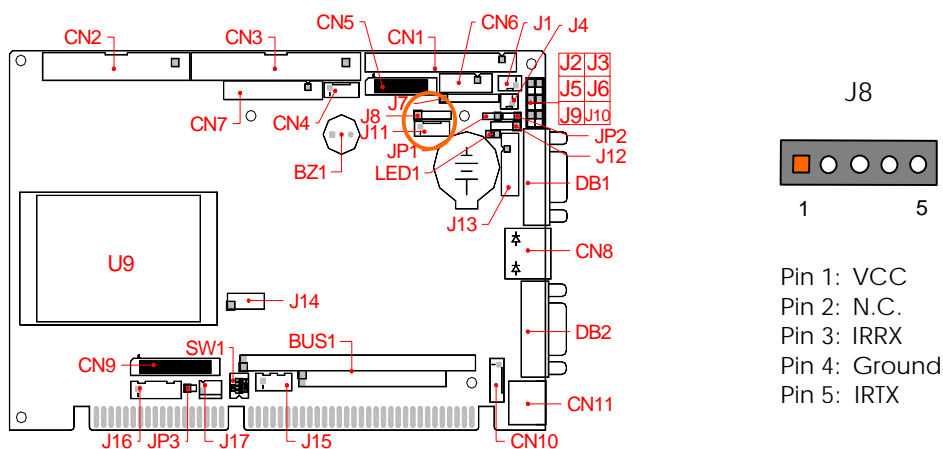
SW1-4	Terminator (422/485)
Off	Off
On	On

Factory Preset: Off

CN6	Signal	RS422	RS485	DB9
1	-DCD2			1
2	-DSR2			6
3	RXD2	RX-	485-	2
4	-RTS2	TX-		7
5	TXD2	RX+	485+	3
6	-CTS2	TX+		8
7	-DTR2			4
8	-RI2			9
9	GROUND			5
10	CASE GROUND			

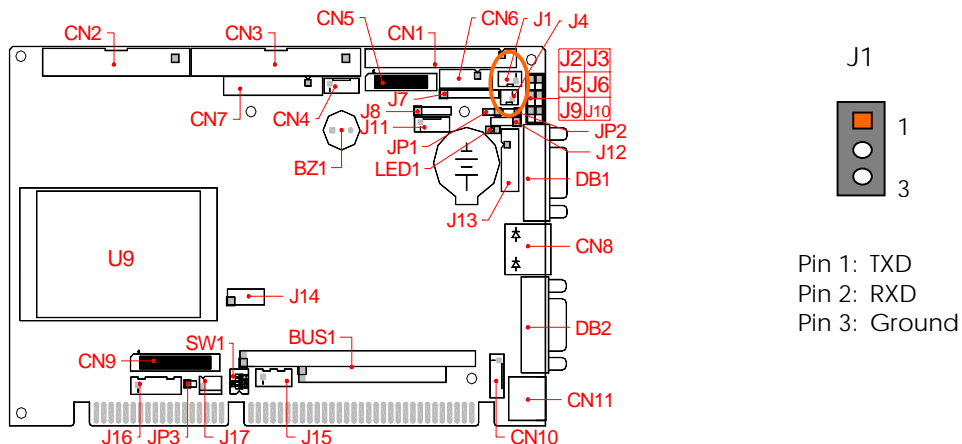
❑ J8: 5-pin Infrared Header

J8 provides infrared signals of serial port 2. The infrared signal is used to interface with Infrared modules.



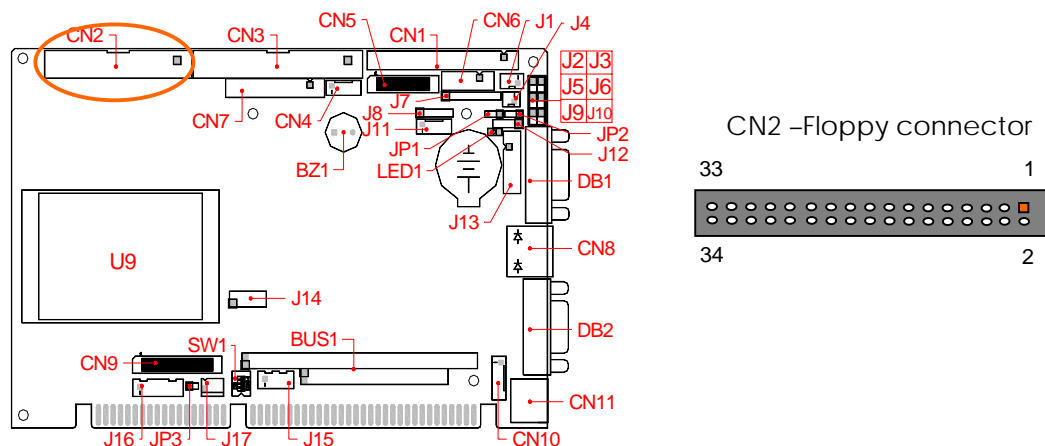
❑ J1: Touch Screen Header

J1 provide basic RS-232C signals of serial port 2 respectively. The basic RS-232C signal is used to interface with touch screen controller internally.



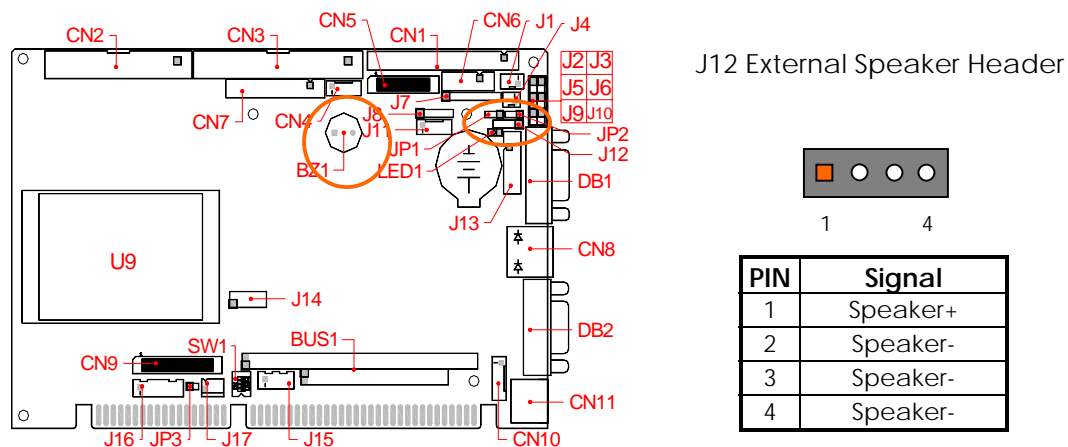
□ CN2: Floppy Connector

The included floppy drive interface cable is used standard 34-pin connector. The following table shows signal connections 34-pin connectors.



34-pin	Signal	34-pin	Signal
2	Drive Enable A	23	Ground
8	-Index	24	-Write Enable
12	-Select A	26	-Track 0
11	Ground	28	-Write Protect
16	-Motor A	29	Ground
14	- Select B	30	-Read Data
10	-Motor B	31	Ground
9	Ground	32	-Head
18	-Direction	33	NC
20	-Step	34	-Disk Change
22	-Write Data	Others	No Connection

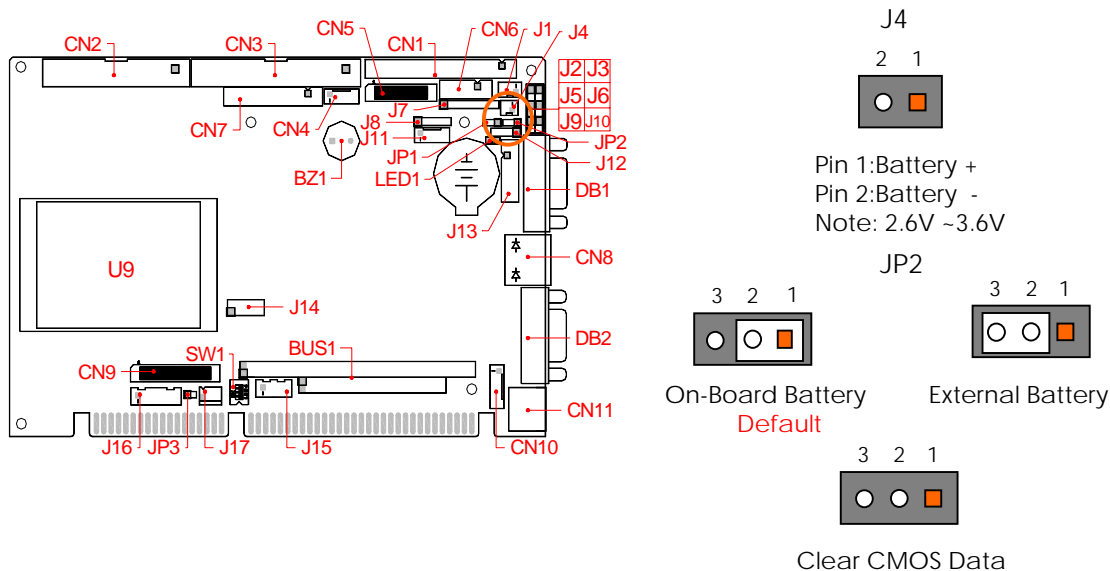
□ BZ1& J12: On-Board Buzzer & External Speaker Header



PIN	Signal
1	Speaker+
2	Speaker-
3	Speaker-
4	Speaker-

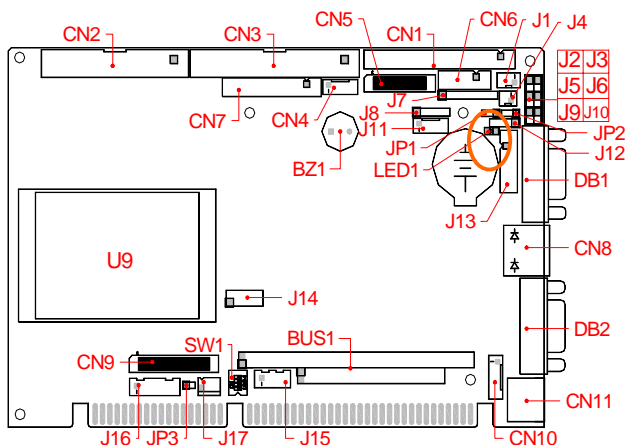
□ J4 & JP2: External Battery Connector and Battery Select Jumper

J4 is used to connect an external battery pack if on-board Lithium battery is empty, and please setting JP2 properly of in-board battery or external battery. You can use JP2 to clear CMOS data. The CMOS store information like system date, time, boot up device, password, IRQ... that are set up with the BIOS. To clear the CMOS, set JP2 to open and then return to 1-2. The default setting is 1-2.



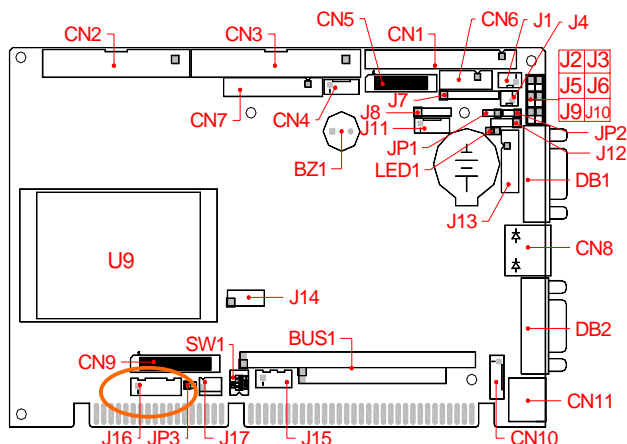
□ On-Board Power and Watchdog LED (LED1)

LED1 indicates power is active when it lights. If the watchdog is enabled, LED1 will blink in a stable period.

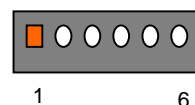


□ **J16: Power Connector (6-pin 2.5mm JST)**

J16 is the power connector for FB2503 is used with stand-alone applications.



J16

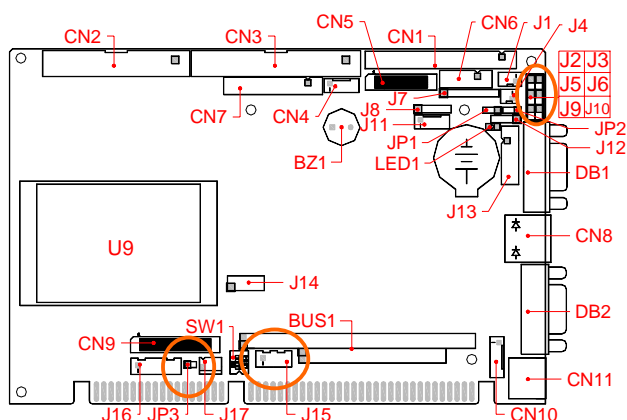


Note: This power connector is ideal for standalone applications.

J16	Signal
1	Ground
2	+5V
3	+5V
4	Ground
5	Ground
6	+12V

□ **J3, J15 & JP3: Soft Start Connector (*for ATX Power Supply Only*)**

When ATX power supply is used, you can connect J15 to ATX control signals from the back plane, and connect J3 to a push bottom switch as soft power switch. If non-ATX power supply is used, please short JP3 with jumper and you don't need to connect J3 and J15.



J3



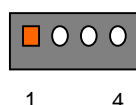
ATX Soft Power Switch Header

JP3



Close: Non - ATX Power
Default
Open: ATX Power

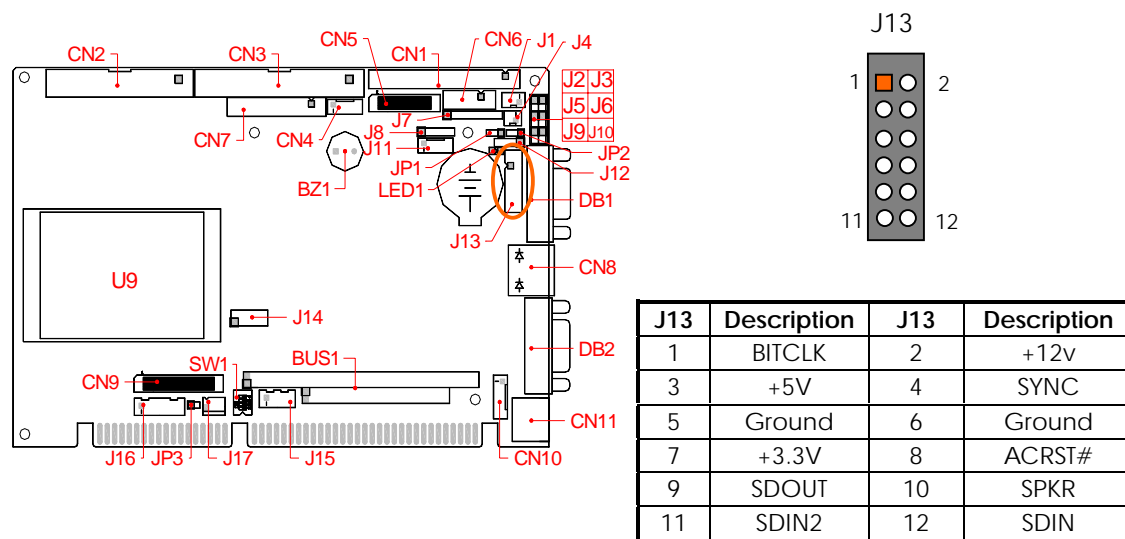
J15



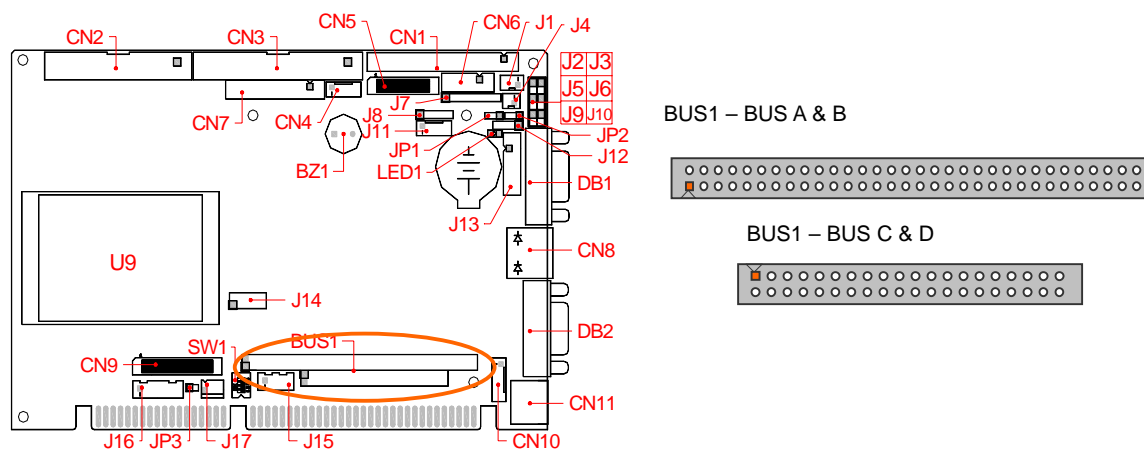
J15	Signal
1	Ground
2	PSON#
3	Power OK
4	VCCSB

□ J13: AMR Connector

J13 provides AC97 signals for Audio and Modem functions. FB4641 (Audio Adapter Board, Optional) is recommended for your best Audio solutions.



□ BUS1: PC/104 Connector



PC/104 A&B Pin

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-IOCHK	A17	SA14	B1	Ground	B17	-DACK1
A2	SD7	A18	SA13	B2	RSTDRV	B18	DRQ1
A3	SD6	A19	SA12	B3	+5V	B19	-REFSH
A4	SD5	A20	SA11	B4	IRQ9	B20	BUSCLK
A5	SD4	A21	SA10	B5	-5V (*1)	B21	IRQ7
A6	SD3	A22	SA9	B6	DRQ2	B22	IRQ6
A7	SD2	A23	SA8	B7	-12V (*1)	B23	IRQ5
A8	SD1	A24	SA7	B8	-ZWS	B24	IRQ4
A9	SD0	A25	SA6	B9	+12V	B25	IRQ3
A10	IORDY	A26	SA5	B10	Key1	B26	-DACK2
A11	AEN	A27	SA4	B11	-MEMW	B27	TC
A12	SA19	A28	SA3	B12	-MEMR	B28	ALE
A13	SA18	A29	SA2	B13	-IOW	B29	+5V
A14	SA17	A30	SA1	B14	-IOR	B30	OSC
A15	SA16	A31	SA0	B15	-DACK3	B31	Ground
A16	SA15	A32	Ground	B16	DRQ3	B32	Ground

PC/104 C& D Pin

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
C1	GND	C11	MEMW#	D1	Ground	D11	-DACK#5
C2	SBHE	C12	SD8	D2	MEMCS16#	D12	DREQ5
C3	LA23	C13	SD9	D3	IOCS16#	D13	DACK#6
C4	LA22	C24	SD10	D4	IRQ10	D14	DREQ6
C5	LA21	C25	SD11	D5	IRQ11	D15	DACK#7
C6	LA20	C26	SD12	D6	IRQ12	D16	DREQ7
C7	LA19	C27	SD13	D7	IRQ15	D17	VCC
C8	LA18	C28	SD14	D8	IRQ14	D18	MASTER#
C9	LA17	C29	SD15	D9	DACK#0	D19	GND
C10	MEMR#	C20	KEY	D10	DREQ0	D20	GND

Chapter 3 Installing CRT & LVDS LCD

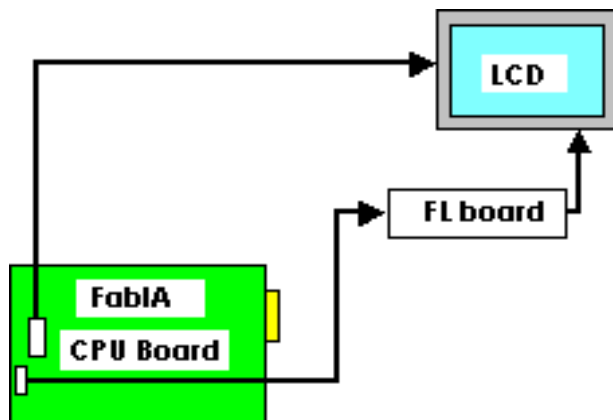
This chapter describes the configuration and installation procedure of LCD and CRT displays. Both CRT and LCD displays may be used at the same time. However, each type of LCD requires different BIOS. This section describes the configuration and installation procedure using LCD display. Skip this section if you are using CRT monitor only.

- LCD Flat Panel Display
- CRT & LCD Display

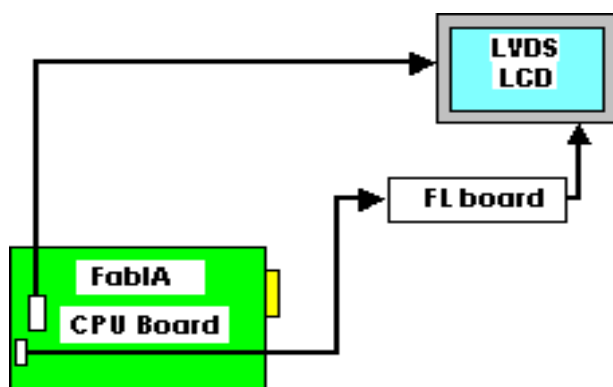
LCD FLAT PANEL DISPLAY

Using the BIOS setting for different types of LCD panel, then set your system properly and configures BIOS setting for the right type of LCD panel you are using.

The following shows the block diagram of using FB2503 for LCD display.



LCD Panel Block Diagram



LVDS/Panel Link Diagram

The block diagram shows that FB2640 till needs components to be used with a LCD panel.

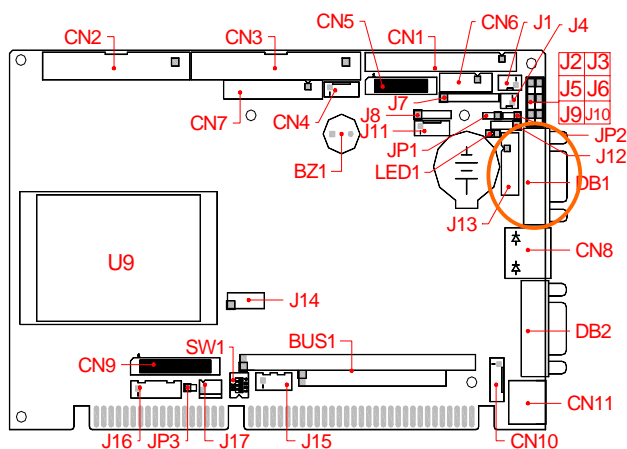
NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable usually has a different color.

CRT & LCD DISPLAY

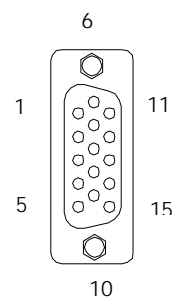
The FB2503 supports a CRT colored monitor and a LCD. It can be connected to create a compact video solution for the industrial environment. 32MB simulated VRAM allows a maximum CRT resolution of 1600X1200 with 64K colors.

DB1: CRT connector

The CRT is use to a standard CRT connector (DB1).



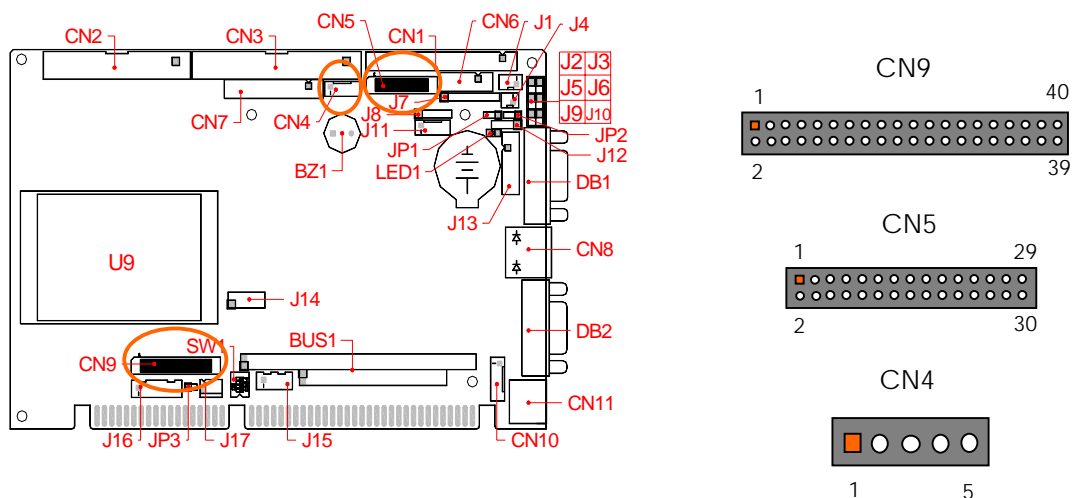
DB1



DB15	Signal	DB15	Signal
1	RED	Case	Case Ground
2	GREEN	5,10	Digital Ground
3	BLUE	6,7,8	Analog Ground
14	VSYNC	15	DDC Clock
13	HSYNC	12	DDC Data

□ **CN9, CN5 & CN4: LCD Connector and Power connector**

CN9 supports 24-bit TTL LCD signals, CN5 supports 36-bit (2 Channel) LVDS LCD signals, and CN4 is the power connector for inverter board.



Pin	CN9	CN5	Pin	CN9	CN5
1	+5V	Ground	2	+5V	Y0+
3	Ground	Y0-	4	Ground	Ground
5	+3.3V	Y1+	6	+3.3V	Y1-
7	NC	Ground	8	Ground	Y2+
9	FP0	Y2-	10	FP1	Ground
11	FP2	YCK+	12	FP3	YCK-
13	FP4	Ground	14	FP5	Z0+
15	FP6	Z0-	16	FP7	Ground
17	FP8	Z1+	18	FP9	Z1-
19	FP10	Ground	20	FP11	Z2+
21	FP12	Z2-	22	FP13	Ground
23	FP14	ZCK+	24	FP15	ZCK-
25	FP16	Ground	26	FP17	Ground
27	FP18	+3.3V	28	FP19	+3.3V
29	FP20	+5V	30	FP21	+5V
31	FP22		32	FP23	
33	Ground		34	Ground	
35	SHFCLK		36	FP (VS)	
37	DE		38	LP (HS)	
39	ENVDD		40	ENAVEE	

Pin	CN4
1	+12 V
2	GND
3	ENABLK
4	N.C
5	+5 V

Note: If any trouble when connecting FB2503 with LCD panels, you could contact technical support division of FabiaTech Corporation.

Chapter 4 BIOS Setup

This chapter describes the BIOS setup.

Overview

BIOS are a program located on a Flash memory chip on a circuit board. It is used to initialize and set up the I/O peripherals and interface cards of the system, which includes time, date, hard disk drive, the PCI bus and connected devices such as the video display, diskette drive, and the keyboard. This program will not be lost when you turn off the system.

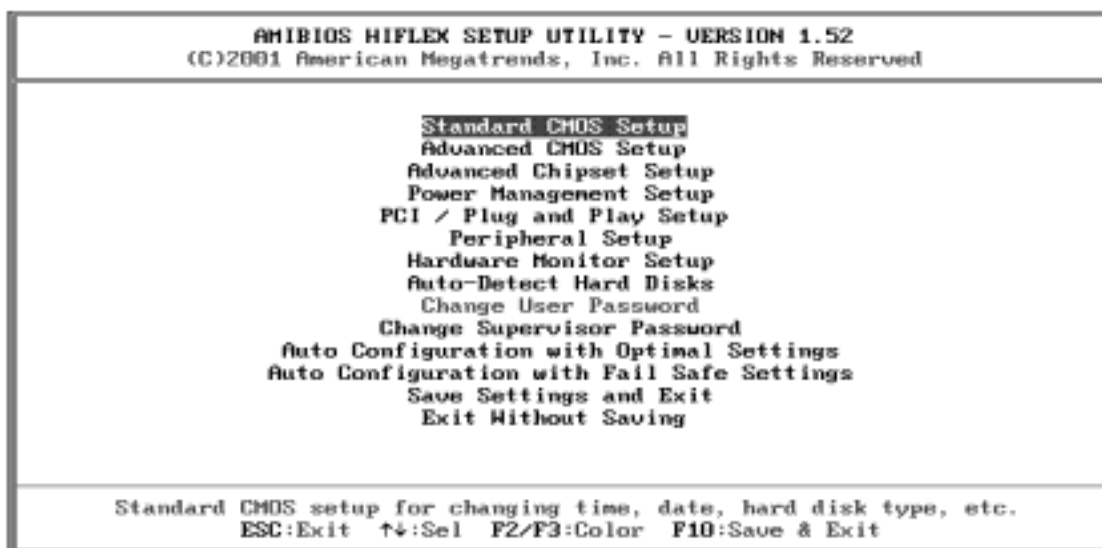
The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation, the user may have corrupted the original settings set by the manufacturer.

All the changes you make will be saved in the system RAM and will not be lost after power-off.

When you start the system, the BIOS will perform a self-diagnostics test called Power on Self Test (POST) for all the attached devices, accessories, and the system. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

Note: Change the parameters when you fully understand their functions and subsequence.



BIOS Functions

On the menu, you can perform the following functions

1. Standard CMOS Setup
2. Advanced CMOS Setup
3. Advanced Chipset Setup
4. Power Management Setup
5. PCI/ Plug and Play Setup
6. Peripheral Setup
7. Hardware Monitor Setup
8. Auto-Detect Hard Disks
9. Change User Password
10. Change Supervisor Password
11. Auto Configuration with Optimal Settings: to auto configure the system according to optimal setting with pre-defined values. This is also the factory default setting of the system when you receive the board.
12. Auto Configuration with Fail Safe Settings: to configure the system in fail-safe mode with predefined values.
13. Save Settings and Exit: perform this function when you change the setting and exit the BIOS Setup program.
14. Exit without saving: perform this function when you want to exit the program and do not save the change.

Keyboard Convention

On the BIOS, the following keys can be used to operate and manage the menu:

Item	Function
ESC	To exit the current menu or message
Page Up/Page Down	To select a parameter
F1	To display the help menu if you do not know the purpose or function of the item you are going to configure
F2/F3	To change the color of the menu display. F2 is to go forward and F3 is to go backward.
UP/Down Arrow Keys	To go upward or downward to the desired item

STANDARD CMOS SETUP

This section describes basic system hardware configuration, system clock setup and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

AMIBIOS SETUP - STANDARD CMOS SETUP									
(C)2001 American Megatrends, Inc. All Rights Reserved									
Date (mm/dd/yyyy): Mon <u>Jan</u> 27, 2003					Base Memory: 0 KB				
Time (hh/mm/ss) : 16:51:04					Extd Memory: 0 MB				
Floppy Drive A: Not Installed									
Floppy Drive B: Not Installed									
	Type	Size	Cyls	Head	WPcom	Sec	LBA Mode	BIk Mode	PIO 32Bit Mode
Pri Master:	Auto								On
Pri Slave :	Auto								On
Sec Master:	Auto								On
Sec Slave :	Auto								On
Boot Sector Virus Protection					Disabled				
Month: Jan - Dec					ESC:Exit ↑↓:Sel				
Day: 01 - 31					PgUp/PgDn:Modify				
Year: 1900 - 2099					F1:Help F2/F3:Color				

□ Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+] / [-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+] / [-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

□ Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

□ Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

❑ **Boot Sector Virus Protection**

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <*Disabled*>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

ADVANCED CMOS SETUP

This section describes the configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

AMIBIOS SETUP - ADVANCED CMOS SETUP		
(C)2001 American Megatrends, Inc. All Rights Reserved		
Quick Boot	Enabled	Available Options: Disabled ▶ Enabled
1st Boot Device	IDE-0	
2nd Boot Device	Floppy	
3rd Boot Device	CD/DVD	
Try Other Boot Devices	Yes	
Hard Disk Access Control	Read-Write	
S.M.A.R.T. for Hard Disks	Disabled	Available Options: ▶ Disabled Enabled
BootUp Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
PS/2 Mouse Support	Enabled	
System Keyboard	Absent	
Password Check	Setup	
Boot To OS/2	No	
Wait For 'F1' If Error	Disabled	
Hit 'DEL' Message Display	Enabled	
L1 Cache	Enabled	
L2 Cache	Enabled	
C800,32k Shadow	Cached	
C800,16k Shadow	Cached	
CC00,16k Shadow	Cached	
D800,16k Shadow	Disabled	
D400,16k Shadow	Disabled	
D000,16k Shadow	Disabled	
DC00,16k Shadow	Disabled	
E800(64k) Shadow Controller	Disabled	ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

□ Quick Boot

This field is used to activate the quick boot function of the system. When set to Enabled,

1. BIOS will not wait for up to 40 seconds if a Ready signal is not received from the IDE drive, and will not configure its drive.
2. BIOS will not wait for 0.5 seconds after sending a RESET signal to the IDE drive.
3. You cannot run BIOS Setup at system boot since there is no delay for the Hit, Del. To run Setup message.

Available Options: Disabled, Enabled

Default setting: Enabled

☐ **1st –3rd Boot Device**

These fields determine where the system attempts to look for the boot drive priority for an operating system. The default procedure is to check the hard disk, and then the floppy drive, and last the CDROM.

Available options: Disabled, IDE0-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CD/DVD, USB-FLOPPY, USB-CDROM, USB-HDD and SCSI, Network

Default setting: IDE-0 for 1st Boot device; Floppy for 2nd Boot Device; CDROM for 3rd Boot Device

☐ **Try Other Boot Device**

If all 3 1st –3rd boot devices specified by CMOS setup are not available to boot, BIOS will try to boot other available devices in following order if this question is set to "Enabled".

☐ **Initial Display Mode**

This field specifies can set Normal POST screen (BIOS) or Boot with logo, no POST messages (Client).

☐ **Floppy Access Control**

This field specifies the read/write access when booting from a floppy drive.

Available options: Normal, Read-only

Default setting: Normal

☐ **Hard Disk Access Control**

This field specifies the read/write access when booting from a HDD drive.

Available options: Normal, Read-only

Default setting: Normal

☐ **S.M.A.R.T for Hard Disk**

This field is used to activate the S.M.A.R.T (System Management and Reporting Technologies) function for S.M.A.R.T HDD drives. This function requires an application that can give S.M.A.R.T message.

Available options: Disabled, Enabled

Default: Disabled

☐ **Boot Up Num-lock**

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Available options: On, Off

Default setting: On

☐ **Floppy Drive Swap**

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of **Disabled** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is **<Enabled>**, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Available options: Disabled, Enabled

Default setting: Disabled

☐ **Floppy Drive Seek**

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.

Available Options: Disabled, Enabled

Default setting: Disabled

☐ **PS/2 Mouse Support**

The setting of **Enabled** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. **Disabled** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Available options: Disabled, Enabled

Default setting: Enable

☐ **System Keyboard**

This field specifies if an error message should be prompted when a keyboard is not attached.

Available options: Absent, Present

Default setting: Absent

☐ **Primary Display**

The field specifies the type of monitor installed in the system.

Available options: Absent, VGA/EGA, CGA40x25, CGA80x25, and Mono

Default setting: Absent

☐ **Password Check**

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Available options: Setup, Always

Default setting: Setup

☐ **Boot To OS2**

If OS2 operating system is used, and the system RAM is over 64MB, please select yes. Otherwise, select No.

Available options: Yes, No

Default setting: No

☐ **Wait for 'F1' If Error**

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this field is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Available options: Disabled, Enabled

Default setting: Disabled

☐ **Hit 'DEL' Message Display**

Set this field to ***Disabled*** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available options: Disabled, Enabled

Default setting: Enabled

❑ **C000, 32k Shadow – E000, 64k shadow**

These fields control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
2. **Enabled:** The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
3. **Cached/WP:** The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Available options: Disabled, Enabled, Cached

Default setting: Disabled

Default setting: Disable

ADVANCED CHIPSET SETUP

This section describes the configuration of the board's chipset features.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
***** DRAM Timing *****		Available Options: ► Disabled Enabled
Configure SDRAM Timing by SPD	Disabled	
DRAM Frequency	100Mhz	
SDRAM CAS# Latency	3	
SDRAM Burst Refresh	Enabled	
Memory Hole	Disabled	
AGP Mode	4x	
AGP Aperture Size	64MB	
ISA Bus Clock	PCICLK/4	
USB Controller	Enabled	
USB Device Legacy Support	All Device	
OnChip VGA Frame Buffer Size	8MB	
Boot Screen Select	CRT	
LCD Panel Type	1	
ATX Power Supply Controller	Disabled	
Power Turn On Time of Delay	Disabled	
Lan Chipset Controller	Enabled	
Lan Boot ROM Controller	Disabled	
		ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

❑ Configure SDRAM Timing by SPD

SPD represents Serial Presence Detect. It is an 8-bit, 2048 bits EEPROM, built on the SDRAM for 100 MHz frequencies. If the installed SDRAM supports SPD function, select SPD. If not, you can select based on other access time of the SDRAM.

Available Options: Disabled, Enabled

Default setting: Disabled

➤ *DRAM Frequency*

This specifies the SDRAM memory clock frequency.

Available Options: 100MHz, 133MHz

Default setting: 100MHz

➤ *SDRAM CAS# Latency (SCLKs)*

This field specifies the latency for the Synchronous DRAM system memory signals.

Available Options: 3, 2

Default setting: 3

☐ **Memory Hole**

This field specifies the location of an area of memory that cannot be addressed on the ISA bus.

Available Options: Disabled, 15MB-16MB, 512KB-64KB

Default setting: Disabled

☐ **AGP Mode**

This field select AGP transfer's video data speed.

Available Options: 1x, 2x and 4x

Default setting: 4x

☐ **AGP Aperture Size**

This field specifies the system memory size that can be used by the Accelerated Graphics Port (AGP).

Available Options: 4MB, 8MB, 16MB, 32MB, 64MB, 128MB and 256MB

Default setting: 64 MB

☐ **USB Control**

Select Enabled if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Enabled

Default setting: Enabled

☐ **USB Device Legacy Support**

Select All Device if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, All Device

Default setting: All Device

☐ **OnChip VGA Frame Buffers Size**

This field is share memory architecture (SMA) for frame buffer memory. SMA allows system memory to be efficiently share by the host CPU and allocated depending on user preference, application requirements, and total size of system memory.

Available Options: None, 2MB, 4MB, 8MB, 16MB and 32MB

Default setting: 8 MB

☐ **Boot Screen Select**

This field specifies which VGA display will be used when the system is boot. You can select either the LCD or the CRT booting on the VGA.

Available Options: Both, LCD, and CRT

Default setting: CRT

☐ **LCD Panel Type**

When use the LCD the field specifies which select display resolution for different TFT and STN LCD display type.

Available Options: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14 and 15

Default setting: 1

LCD Panel Type Table

Panel ID	Function	CN6	CN5
0	640x480	TFT	
1	800x600	TFT	LVDS
2	1024x768 2 Pixel/Clk at 32Mhz	TFT	
3	1280x1024	TFT	
4	640x480	DSTN	
5	800x600	DSTN	
6	1600x1200	TFT	LVDS
7	1024x768 1 Pixel/Clk at 65Mhz	TFT	
8	640x480	TFT	LVDS
9	800x600	TFT	
10	1024x768	TFT	
11	1280x1024	TFT	
12	1400x1050 2 Pixel/Clk at 54Mhz	TFT	
13	800x600	TFT	
14	1024x768	DSTN	
15	1280x1024	DSTN	

☐ **LAN Chipset Controller**

This field specifies the Enable or Disable of the onboard LAN chip.

Available Options: Disabled, Enable

Default setting: Enable

☒ **LAN Boot ROM Controller**

This field specifies the PXE boot ROM of the onboard LAN chip.

Available Options: Disabled, Enable

Default setting: Disable

POWER MANAGEMENT

AMIBIOS SETUP - POWER MANAGEMENT SETUP		
(C)2001 American Megatrends, Inc. All Rights Reserved		
ACPI Aware O/S	No	Available Options: ▶ Disabled Enabled
Power Management/APM	Disabled	
Video Power Down Mode	Disabled	ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color
Hard Disk Power Down Mode	Disabled	
Standby Time Out (Minute)	Disabled	
Suspend Time Out (Minute)	Disabled	
Throttle Slow Clock Ratio	50%-56.25%	
Display Activity	Ignore	
IRQ3	Monitor	
IRQ4	Monitor	
IRQ5	Ignore	
IRQ7	Monitor	
IRQ9	Ignore	
IRQ10	Ignore	
IRQ11	Ignore	
IRQ13	Ignore	
IRQ14	Monitor	
IRQ15	Ignore	
Resume On RTC Alarm	Disabled	
RTC Alarm Date	15	
RTC Alarm Hour	12	
RTC Alarm Minute	30	
RTC Alarm Second	30	

☐ ACPI Aware O/S

This field specifies allow you enable Advanced Configuration and Power Management. When you use Windows/OS standby mode can set to enable.

Available Options: Disabled, Enabled

Default setting: Disable

☐ Power Management /APM

Select Enabled to activate the chipset Power Management and APM (Advanced Power Management) features.

Available Options: Disabled, Enabled

Default setting: Enabled

☐ Video Power Down Mode

This field specifies the power conserving state that video subsystem enters after the specified period of display inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

☐ **Hard Disk Power Down Mode**

This field specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

☐ **Standby Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in full power on state. When this length of time expires, the system enters Standby power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

☐ **Suspend Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in Standby state. When this length of time expires, the system enters Suspend power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

☐ **Throttle Slow Clock Ratio**

When the system enter Suspend or standby mode, the CPU clock runs only part of the time. You may select the percent of time that the clock runs.

Available Options: 0%-6.25, 25%37.5%, 75%87.5% and 93.75%-100%

Default setting: 50%-56.25%

☐ **IRQ3 ~IRQ15**

This field specifies the power down mode of the system based on the device. When the system does not receive signals from the device, it will enter the Power Down mode immediately. To enable the power saving mode, select Monitor. To disable it, select Ignore.

☐ **Resume On RTC Alarm**

This field specifies the RTC alarm to be turned off by extra software.

Available Options: Disabled, Enabled

Default setting: Disabled

☐ **RTC Alarm Date**

This field specifies the date of the RTC alarm.

Available Options: 1, 31

Default setting: 15

☐ **RTC Alarm Hour**

This field specifies the hour of the RTC alarm.

Available Options: 1-24

Default setting: 12

☐ **RTC Alarm Minute**

This field specifies the minute of the RTC alarm.

Available Options: 1-60

Default setting: 30

☐ **RTC Alarm Second**

This field specifies the second of the RTC alarm.

Available Options: 1-60

Default setting: 30

PCI/PLUG AND PLAY

AMIBIOS SETUP - PCI / PLUG AND PLAY SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	No	Available Options: ▶ 32 64 96 128 160 192 224 248
Clear NURAM	No	
PCI Latency Timer (PCI Clocks)	32	
Primary Graphics Adapter	PCI	
PCI UGA Palette Snoop	Disabled	
Allocate IRQ to PCI UGA	No	
PCI IDE BusMaster	Disabled	
DMA Channel 0	PnP	
DMA Channel 1	PnP	
DMA Channel 3	PnP	
DMA Channel 5	PnP	
DMA Channel 6	PnP	
DMA Channel 7	PnP	
IRQ3	PCI/PnP	
IRQ4	PCI/PnP	
IRQ5	PCI/PnP	
IRQ7	PCI/PnP	
IRQ9	PCI/PnP	
IRQ10	PCI/PnP	
IRQ11	PCI/PnP	
IRQ14	PCI/PnP	
IRQ15	PCI/PnP	
		ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

☐ Plug and Plug Aware O/S

Set to Yes to inform BIOS that the operating system can handle Plug and Play (PnP) devices.

Available Options: Yes, No

Default setting: No

☐ PCI Latency Timer

This field specifies the latency timings (in PCI clock) PCI devices installed in the PCI expansion bus.

Available Options: 32, 64, 96, 128, 160, 192, 224, and 248

Default setting: 64

☐ Primary Graphics Adapter

This field specifies which VGA display will be used when the system is boot. You can select either the onboard AGP or the VGA card installed on the PCI bus.

Available Options: AGP, PCI

Default setting: PCI

☐ **PCI VGA Palette Snoop**

When Enabled is selected, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit. (0 is disabled).

Available Options:

Disabled: Data read and written by the CPU is only directed to the PCI VGA devices palette registers.

Enabled: Data read and written by the CPU is directed to both the PCI VGA devices palette registers.

Default setting: Disable

☐ **Allocate IRQ to PCI AGP**

When a PCI or AGP VGA device is installed, you can assign an IRQ to this device. Selecting Yes, BIOS will auto-assign IRQ to the device. Selecting No, no IRQ will be assigned to the VGA device.

Available Options: Yes, No

Default setting: No

☐ **PCI IDE BusMaster**

This option is to specify that the IDE controller on the PCI local bus have bus-mastering capability.

Available Options: Enable, Disable

Default setting: Disable

☐ **DMA Channel 0 – 7**

When I/O resources are controlled manually, you can assign each system DMA as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

Available Options: PnP, ISA/EISA

Default setting: PnP

❑ **IRQ 3 –15**

When I/O resources are controlled manually, you can assign each system interrupt as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

PERIPHERAL SETUP

This section describes the function of peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Auto	Available Options: ▶ Auto Disabled Enabled
OnBoard Serial Port1	Auto	
OnBoard Serial Port2	Auto	
OnBoard Parallel Port	Auto	
Parallel Port Mode	Normal	
EPP Version	N/A	
Parallel Port DMA Channel	N/A	
Parallel Port IRQ	Auto	
OnBoard IDE	Both	
IDE Connection Cable	40-Pin	
OnBoard AC'97 Audio	Enabled	ESC:Exit F1:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color
OnBoard Legacy Audio	Disabled	
Sound Blaster	Disabled	
SB I/O Base Address	220h-22Fh	
SB IRQ Select	5	
SB DMA Select	1	

❑ OnBoard FDC

This field enables the floppy drive controller on the FB2503.

Available Options: Disabled, Enabled and Auto

Default setting: Auto

❑ OnBoard Serial Port 1

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: Auto

❑ OnBoard Serial Port 2

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: Auto

❑ **OnBoard Parallel Port**

This field selects the I/O port address for parallel port.

Available Options: Auto, Disabled, 378, 278, and 3BCH

Default setting: Auto

➤ ***EPP Version***

This field specifies the EPP version for the Parallel Port Mode specification used in the system and is not configurable. IF Normal or ECP is selected, this field displays N/A, meaning not available.

Available Options: N/A, 1.7, 1.9

Default setting: N/A

➤ ***Parallel Port Mode***

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

Available Options: N/A, Normal, Bi-Dir, EPP, and ECP

Default setting: Normal

➤ ***Parallel Port IRQ***

This field specifies the IRQ for the parallel port.

Available Options: Auto, N/A, 5, 7

Default setting: Auto

➤ ***Parallel Port DMA Channel***

This option is only available if the setting for the parallel Port Mode option is ECP.

Available Options: N/A, 0,1,3

Default setting: N/A

❑ **On-Board IDE**

This field specifies the IDE channel that can be applied when using CN3 IDE hard disk connector.

Available Options: Disabled, Primary, and Secondary, Both

Default setting: Both

➤ **IDE Connection Cable**

This field specifies the select IDE use 40-pin or 40pin-80 conductor cable that can be applied when using UltraDMA/66/100 devices on CN3 IDE hard disk connector.

Available Options: 40-pin, 80-pin

Default setting: 40-pin

❑ **OnBoard AC'97 Audio**

This field specifies the internal Audio Control.

Available Options: Disable, Enable

Default setting: Enable

➤ **Sound Blaster**

This field if you want to use the Sound Blaster emulation feature.

Available Options: Disable, Enable

Default setting: Disable

◆ **SB I/O Base Address**

These fields select the I/O port address for Audio.

Available Options: 220H~22FH, 240H~24FH, 260H~26FH and 280~28FH

Default setting: 220H~22FH

◆ **SB IRQ Select**

This field specifies the IRQ for the Audio.

Available Options: Disable, 5,7 and 10

Default setting: 5

◆ **SB DMA Select**

This field specifies the DMA for internal Audio Control.

Available Options: Disable, 0, 1,2 and 3

Default setting: 1

Hardware Monitor Setup

On the Hardware Monitor Setup screen, you can set up or monitor the system temperature, CPU voltage, and VIA C3 CPU Ration and CPU fan speed...

AMIBIOS SETUP - HARDWARE MONITOR SETUP	
(C)2001 American Megatrends, Inc. All Rights Reserved	
-== System Hardware Monitor ==-	
Current CPU Temperature	
Current Ext. Temperature	
Fan1 Speed	0 RPM
CPU VCORE	+1.125V
CPU VTT	+1.500V
+ 3.300V	+3.359V
+ 5.000V	+4.975V
+12.000V	+12.077V
ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color	

□ System Hardware Monitor

In this field, you can monitor or detect the followings items. These items are view-only and cannot be changed.

- Current CPU Temperature
- Current Ext. Temperature
- Fan1 Speed
- CPU1 VCORE
- CPU VTT
- +3.300V
- +5.000V
- +12.00V

Password Setup

There are two security passwords: Supervisor and User. Supervisor is a privileged person that can change the User password from the BIOS.

According to the default setting, both access passwords are not set up and are only valid after you set the password from the BIOS.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Type the desired password (up to 8 character length) when you see the message, "Enter New Supervisor Password."
3. Then you can go on to set a user password (up to 8 character length) if required. Note that you cannot configure the User password until the Supervisor password is set up.
4. Enter Advanced CMOS Setup screen and point to the Password Checkup field.
5. Select Always or Setup.
 - ✧ **Always:** a visitor who attempts to enter BIOS or operating system will be prompted for password.
 - ✧ **Setup:** a visitor who attempts to the operating system will be prompted for user password. You can enter either User password or Supervisor password.
6. Point to **Save Settings and Exit** and press Enter.
7. Press Y when you see the message, "Save Current Settings and Exit (Y/N)?"

Note: it is suggested that you write down the password in a safe place to avoid that password may be forgotten or missing.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Press Enter instead of entering any character when you see the message, "Enter New Supervisor Password."
3. Thus you can disable the password.

Chapter 5 Driver and Utility

The enclosed diskette includes FB2503 VGA driver and LAN driver.

VIA 4 In 1 Driver

WIN 98/2000/XP Driver

Installs VIA Chipset, IRQ Routing, AGP Driver and PCI IDE Bus Master 4in 1Driver.

- 1 To install the VIA 4 IN 1 driver, insert the CD ROM into the CD ROM device, and enter DRIVER>SysChip>VIA4IN1. If your system is not equipped with a CD ROM device, copy the VIA 4 IN 1 driver from the CD ROM to CF or USB Device.
- 2 Execute VIAHyperion4in1XXXX.exe file.
- 3 The screen shows the SETUP type. Press any key to enter the main menu.
- 4 As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

VGA Driver for WIN98/ME

- Step 1: To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>VGA>Via8606>Win98_Me.
- Step 2: Open the Control Panel and double-click "SYSTEM" icon and then Click the "DEVICE Manager" Tab and double click "VGA Display".
- Step 3: Click on DRIVE from the menu bar and new screen appears with the "Update Driver" button and then system will search VGA drive file starting form CD ROM drive.
- Step 4: As the installation is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

- Step 5: In the WINDOWS98/ME, you can find the <DISPLAYL> icon located in the {CONTROL PANEL} group.
- Step 6: Adjust the <Refresh Rate>, and <Resolution>.

Note: In the VGA >Via8606>WINXP_2K directory, a Install.txt file is included to provide installation information

Audio Drivers

WIN 98_ME/WINXP_2K Driver

- 1 To install the AUDIO driver, insert the CD ROM into the CD ROM device, and enter DRIVER>AUDIO>Vt686B. If your system is not equipped with a CD ROM device, copy the Audio driver from the CD ROM to CF.
- 2 Execute SETUP.exe file.
- 3 The screen shows the SETUP type. Press any key to enter the main menu.
- 4 As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

BIOS Flash Utility

In the <UTILITY> directory, there is the FLASH845.EXE file.

Step 1: Use the AMIFLASH.COM program to update the BIOS setting.

Step 2: And then refer to the chapter "BIOS Setup", as the steps to modify BIOS.

Step 3: Now the CPU board's BIOS loaded with are the newest program; user can use it to modify BIOS function in the future, when the BIOS add some functions.

LAN Utility

Step 1: To install the LAN utility OR driver, insert the CD ROM into the CD ROM device, and enter DRIVER>LAN>RTL8139C>DIAG. If your system is not equipped with a CD ROM device, copy the LAN driver from the CD ROM to a 1.44" diskette.

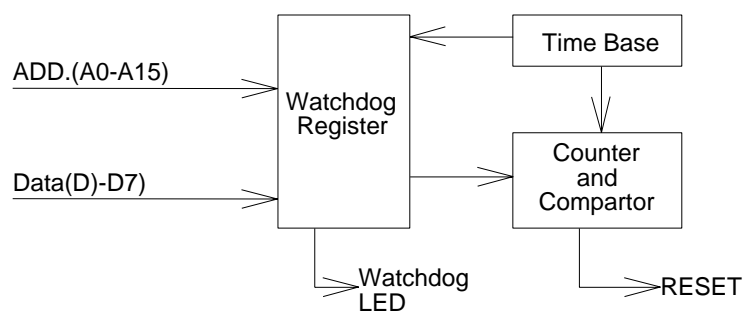
Step 2 Execute install.exe file.

Note: In the RTL8139C directory, a HELPM.EXE file is included to provide installation information

Watchdog Timer

This section describes how to use the Watchdog Timer, including disabled, enabled, and trigger functions.

The FB2503 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be set from 3 to 46 seconds.



Note: If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period. And if you use the IRQ15 signal to warn your program when watchdog timer out, please enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard ISA IDE> and <IDE Prefetch> these two items must set to *Primary*.

Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect system crashes or hang-ups. LED1 on this CPU board is the watchdog timer indicator, which is located at the upper-left corner above the USB connector. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, it will be set to non-zero value to watchdog counter and start to count down again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 8 timer factors. If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Reset Time Factor	IRQ 11 Time Factor	IRQ 15 Time Factor	Time-Out Period (Sec)
20h	38h	30h	3
21h	39h	31h	9
22h	3Ah	32h	15
23h	3Bh	33h	22
24h	3Ch	34h	28
25h	3Dh	35h	34
26h	3Eh	36h	40
27h	3Fh	37h	46

Note:

1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.
2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously; otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 76H. The following is a BASICA program, which demonstrates how to enable the watchdog timer and set the time-out period at 28 seconds.

```
1000      REM Points to command register
1010      WD_REG% = 76H
1020      REM Timer factor = 24H (or 34H)
1030      TIMER_FACTOR% = %H24
1040      REM Output factor to watchdog register
1050      OUT WD_REG%, TIMER_FACTOR%
```

Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program, which demonstrates how to trigger the watchdog timer:

```
2000      REM Points to command register
2010      WD_REG% = 76H
2020      REM Timer factor = 76H (or 34H)
2030      TIMER_FACTOR% = &H76
2040      REM Output factor to watchdog register
2050      OUT WD_REG%, TIMER_FACTOR%
      . Etc.
```

Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000      REM Points to command register
3010      WD_REG% = BASE_PORT%
3020      REM Timer factor = 0
3030      TIMER_FACTOR% = 0
3040      REM Output factor to watchdog register
3050      OUT WD_REG%, TIMER_FACTOR%
      . Etc.
```

Programming RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 precedes the transmission, which needs control the TXC signal, and the installing, steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

Note: Please refer to the section of the "Serial Ports" in the Chapter "Technical Reference" for the detail description of the COM port's register.

❑ **Initialize COM port**

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the FB2503 CPU card's DTR signal to the RS-485' s TXC communication.

❑ **Send out one character (Transmit)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

❑ **Send out one block data (Transmit – the data more than two characters)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

❑ **Receive data**

The RS-485's operation of receiving data is in the same of the RS-232's.

❑ **Basic Language Example**

a. Initial 86C450 UART

```

10      OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20      REM Reset DTR
30      OUT &H3FC, (INP(%H3FC) AND &HFA)
40      RETURN

```

b. Send out one character to COM1

```

10      REM Enable transmitter by setting DTR ON
20      OUT &H3FC, (INP(&H3FC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H3FD) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H3FC, (INP(&H3FC) AND &HEF)
90      RETURN

```

❑ **c. Receive one character from COM1**

```

10      REM Check COM1: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
50      RETURN

```

```
60      REM Read one character from COM1: buffer
70      INPSTR$=INPUT$(1,#1)
80      RETURN
```

NOTE: The example of the above program is based on COM1 (I/O Address 3F8h).
The RS-485 of the FB2503 uses COM2. If you want to program it, please refer to
the BIOS Setup for COM2 address setup.

Chapter 6 Technical Reference

This section outlines the errors that may occur when you operate the system, and also gives you the suggestions on solving the problems.

Topic include:

- Trouble Shooting for Error Messages
- Technical Reference

Trouble Shooting for Error Messages

The following information informs the error messages and troubleshooting. Please adjust your systems according to the messages below. Make sure all the components and connectors are in proper position and firmly attached. If the errors still exist, please contact with your distributor for maintenance.

❑ POST BEEP

Currently there are two kinds of beep codes in BIOS setup.

- One indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by three short beeps.
- The other indicates that an error has occurred in your DRAM. This beep code consists of a constant single long beep.

❑ CMOS BATTERY FAILURE

When the CMOS battery is out of work or has run out, the user has to replace it with a new battery.

❑ **CMOS CHECKSUM ERROR**

This error informs that the CMOS has corrupted. When the battery runs weak, this situation might happen. Please check the battery and change a new one when necessary.

❑ **DISPLAY SWITCH IS SET INCORRECTLY**

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in BIOS Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter BIOS Setup and change the video selection.

❑ **DISK BOOT FAILURE**

When you can't find the boot device, insert a system disk into Drive A and press < Enter >. Make sure both the controller and cables are all in proper positions, and also make sure the disk is formatted. Then reboot the system.

❑ **DISKETTE DRIVES OR TYPES MISMATCH ERROR**

When the diskette drive type is different from CMOS, please run setup or configure the drive again.

❑ **ERROR ENCOUNTERED INITIALIZING HARD DRIVE**

When you can't initialize the hard drive, ensure the following things:

1. The adapter is installed correctly
2. All cables are correctly and firmly attached
3. The correct hard drive type is selected in BIOS Setup

❑ **ERROR INITIALIZING HARD DISK CONTROLLER**

When this error occurs, ensure the following things:

1. The cord is exactly installed in the bus.
2. The correct hard drive type is selected in BIOS Setup
3. Whether all of the jumpers are set correctly in the hard drive

❑ **FLOPPY DISK CONTROLLER ERROR OR NO CONTROLLER PRESENT**

When you cannot find or initialize the floppy drive controller, please ensure the controller is in proper BIOS Setup. If there is no floppy drive installed, ensure the Diskette Drive selection in Setup is set to NONE.

❑ **KEYBOARD ERROR OR NO KEYBOARD PRESENT**

When this situation happens, please check keyboard attachment and no keys being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in BIOS Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot procedure.

❑ **MEMORY ADDRESS ERROR**

When the memory address indicates error. You can use this location along with the memory map for your system to find and replace the bad memory chips.

❑ **MEMORY SIZE HAS CHANGED**

Memory has been added or removed since last boot. In EISA mode, use Configuration Utility to re-configure the memory configuration. In ISA mode enter BIOS Setup and enter the new memory size in the memory fields.

❑ **MEMORY VERIFYING ERROR**

It indicates an error verifying a value is already written to memory. Use the location along with your system's memory map to locate the bad chip.

❑ **OFFENDING ADDRESS MISSING**

This message is used in connection with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

❑ **REBOOT ERROR**

When this error occurs that requires you to reboot. Press any key and the system will reboot.

❑ **SYSTEM HALTED**

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Technical Reference

Real-Time Clock and Non-Volatile RAM

The FB2503 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM.

Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte

Address	Description
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

CMOS RAM Map

Register	Description
00h -10h	Standard AT-compatible RTC and Status and Status Register data definitions
11h – 13h	Varies
14h	<p>Equipment</p> <p>Bits 7-6 Number of Floppy Drives</p> <p>00 1 Drive</p> <p>01 2 Drives</p> <p>Bits 5-4 Monitor Type</p> <p>00 Not CGA or MDA 01 40x25 CGA</p> <p>01 2 Drives 80x25 CGA</p> <p>Bits 3 Display Enabled</p> <p>0 Disabled</p> <p>1 Enabled</p> <p>Bit 2 Keyboard Enabled</p> <p>00 Not CGA or MDA 01 40x25 CGA</p> <p>01 2 Drives 80x25 CGA</p> <p>Bit 1 Math Coprocessor Installed</p> <p>0 Absent</p> <p>1 Present</p> <p>Bit 0 Floppy Drive Installed</p> <p>0 Disabled</p> <p>1 Enabled</p>
15h	Base Memory (in 1KB increments), Low Byte
16h	Base Memory (in 1KB increments), High Byte
17h	IBM-compatible memory (in 1KB increments), Low Byte
18h	IBM-compatible memory (in 1KB increments), High Byte (max 15 MB)
19h-2Dh	Varies
2Eh	Standard CMOS RAM checksum, high byte
2Fh	Standard CMOS RAM checksum, low byte
30h	IBM-compatible Extended Memory, Low Byte (POST) in KB
31h	IBM-compatible Extended Memory, High Byte (POST) in KB
32h	Century Byte
33h	Reserved. Do not use
34h	Reserved. Do not use
35h	Low byte of extended memory (POST) in 64 KB
36h	High byte of extended memory (POST) in 64 KB
37h-3Dh	Varies
3Eh	Extended CMOS Checksum, Low Byte (including 34h-3Dh)
3Fh	Extended CMOS Checksum, High Byte (including 34h-3Dh)

I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. There is a total of 1K-port address space available. The following table lists the I/O port addresses used on the Industrial CPU Card.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h - 0FFh	Math Coprocessor
1F0h - 1F7h	IDE Interface
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
378h - 3FFh	Parallel Port #1(LPT1)
3B0h - 3BFh	Monochrome & Printer adapter
3C0h - 3CFh	EGA adapter
3D0h - 3DFh	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)
400h - 40Fh	Plug & Play ISA Bus
4D5h - 4D1h	Plug & Play ISA Bus
800h - 87Fh	Plug & Play ISA Bus
880h - 88Fh	Plug & Play ISA Bus
C00h - CFFh	Plug & Play ISA Bus
CF8h - CFFh	Plug & Play ISA Bus
E800h - E8FEh	Ethernet Controller
EC00h - EC1Eh	USB Controller
FC00h - FC0Eh	IDE Controller

Interrupt Request Lines (IRQ)

There are a total of 15 IRQ lines available on the Industrial CPU Card. Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on the Industrial CPU Card.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	USB
IRQ11	Ethernet
IRQ12	PS2 Mouse
IRQ13	Math coprocessor
IRQ14	Primary IDE
IRQ15	Secondary IDE

DMA Channel Map

The equivalent of two 8237A DMA controllers are implemented in the FB2503 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Serial Ports

The ACEs (Asynchronous Communication Elements ACE1 to ACE2) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

❑ Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

❑ Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

❑ Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

❑ **Interrupt Identification Register (IIR)**

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

❑ **Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

❑ **MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

❑ **Line Status Register (LSR)**

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

❑ **MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

□ **Divisor Latch (LS, MS)**

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Parallel Ports

❑ Register Address

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

❑ Printer Interface Logic

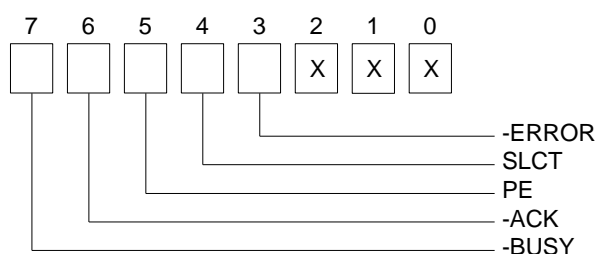
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

❑ Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address

❑ Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

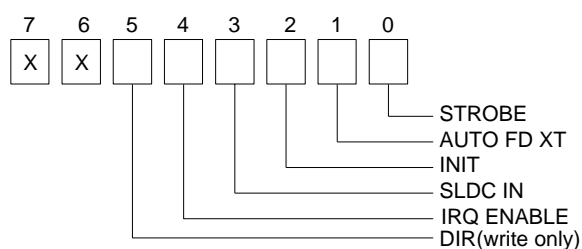


NOTE: X represents not used.

- Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.
- Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.
- Bit 5: A 1 means the printer has detected the end of the paper.
- Bit 4: A 1 means the printer is selected.
- Bit 3: A 0 means the printer has encountered an error condition.

❑ Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

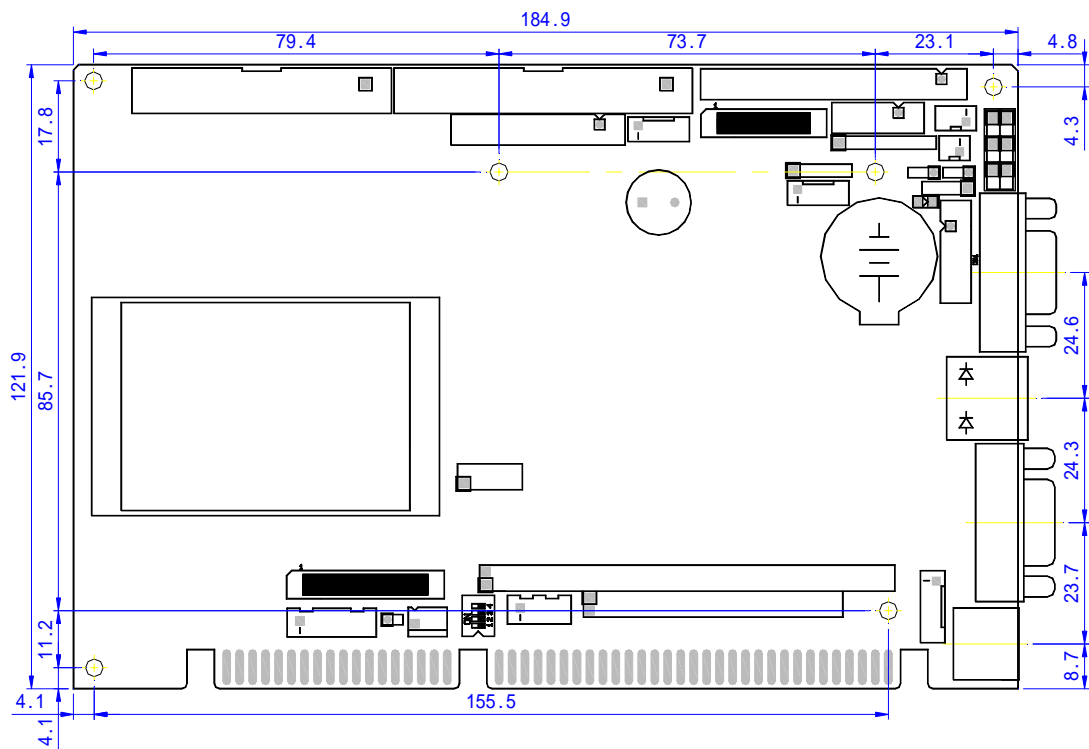


NOTE: X represents not used.

- Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write-only.
- Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.
- Bit 3: A 1 in this bit position selects the printer.
- Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).
- Bit 1: A 1 causes the printer to line-feed after a line is printed.
- Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

Appendix

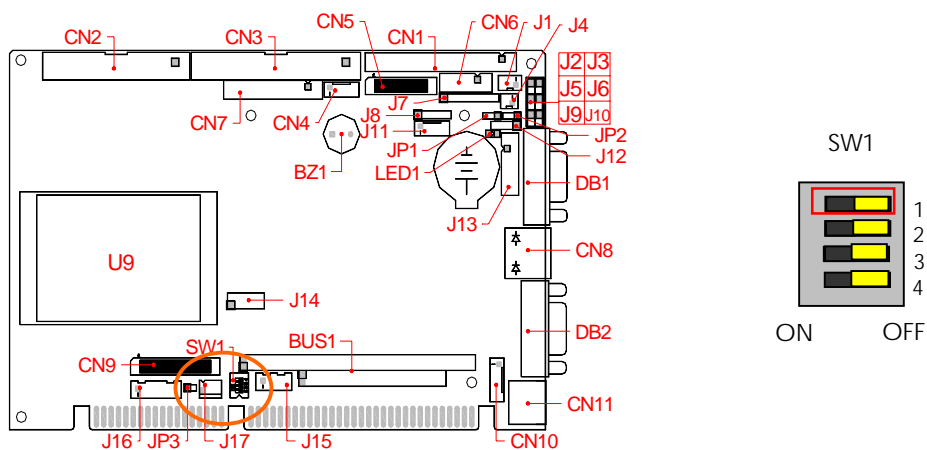
A: Dimension



Unit: mm

B: SRAM

If SRAM is to be used, select a mapping memory address for it. Two addresses are provided, D400, D800. The default setting is D800.



SW1-1	U23	Remark
On	D400h:0	
Off	D800h:0	Factory Present

➤ SRAM memory banks

This provides the information about how to access the memory on the FB2503. The FB2503 hardware divides every 8K bytes of memory into a memory bank. To access the data in the memory, you have to assign a bank number. The memory bank number starts from zero. The last memory bank number depends on the size of the memory chip used on the FB2503. For example, if you use the 128K bytes memory chip, the bank number would be in the range of 0 to 15.

The I/O port address of the bank select base port 84ch or 84dh, the following is the format of the chip select and bank enable.

Register	I/O Port	D7	D6	D5	D4	D3	D2	D1	D0
Bank select	84ch	-	-	BNK5	BNK4	-	-	-	Sel1
Bank select	84dh		-	-	-	BNK3	BNK2	BNK1	BNK0

SRAM	Sel1
U23	0
Disable	1

Where:

Sel1 Select the SRAM CHIP's

BNK4~bnk5 Bank select bits, D0 is the LSB

NOTE: Bnk0 to Bnk5 are the memory bank select bits. For example, 128KB memory has sixteen 8K-byte banks; so 4 bits (Bnk0 to Bnk3) are needed.

Example: Select the 10th bank of the U23 on the FB2503. Using 128K*8, and the base port is &H84c.

100 base_port=&H84c

110 OUT base_port,&H00

120 base_port=&H84d

130 base_port=&H09