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FB2642 Socket 370 PIII / Celeron Half-size CPU Card User's Manual

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- ❑ A list of your name, address, telephone, facsimile number, or email address where you may be reached during the day
- ❑ Description of you peripheral attachments
- ❑ Description of you software (operating system, version, application software, etc.) and BIOS configuration
- ❑ Description of the symptoms (Extract wording any message)

For updated BIOS, drivers, manuals, or product information, please visit us at www.fabiatech.com

Table of Content

FB2642 Socket 370 PIII / Celeron Half-size CPU Card User's Manual	i
Table of Content	iii
Chapter 1 Introducing theFB2642 System Board.....	1
Overview	1
Layout	2
Specifications	3
Packing List	4
Chapter 2 Hardware Installation	5
Before Installation	5
Hardware Features	6
SW1 (3,4): Selecting CPU Base Clock and PCI Clock	7
J1 & J5: CPU Fan Connector & System Fan Connector	8
J2: USB Connector	8
J13: Reset Header.....	9
J9: Power LED Header.....	9
J11: HDD LED Header.....	9
CN2, CN3: Keyboard/Mouse Connector	10
CN5: RJ45 LAN Connector	10
CN8, CN9: IDE hard Disk Connector.....	11
DB1 & CN4: RS232 Serial Ports 1,2 Connectors and Jumpers.....	12
CN6: 26-pin Parallel Port Connector.....	14
CN7: Floppy Connector	15
BZ1 & J10: On-Board Buzzer & External Speaker Header	15
J7: Temperature Sensor Header	16
JP1: CMOS Data Clear Jumper.....	16
LED1:On-Board Power LED	16

J6: TTL I/O Connector.....	17
CN1: Power Connector (9-pin 2.54mm JST)	17
J8: External TX-LED with LAN LED Header.....	18
DB2: CRT connector.....	18
Chapter 3 BIOS Setup	19
Overview.....	19
BIOS Functions.....	20
Keyboard Convention.....	21
STANDARD CMOS SETUP	22
ADVANCED CMOS SETUP	24
ADVANCED CHIPSET SETUP.....	29
POWER MANAGEMENT	32
PCI/PLUG AND PLAY.....	34
PERIPHERAL SETUP	37
Hardware Monitor Setup	40
Password Setup.....	41
Chapter 4 Driver and Utility	43
VGA Driver for WIN98/WIN95	43
BIOS Flash Utility.....	44
LAN Utility.....	44
Watchdog Timer	45
Watchdog Timer Setting	46
Watchdog Timer Enable & Trigger	47
Watchdog Timer Disabled.....	48
Programming RS-485	48
Chapter 5 Technical Reference	53
Trouble Shooting for Error Messages	53
Technical Reference.....	56
Real-Time Clock and Non-Volatile RAM.....	56
CMOS RAM Map	58
I/O Port Address Map.....	59
Interrupt Request Lines (IRQ)	60
DMA Channel Map.....	61
DMA Controller 2.....	61

Serial Ports.....	62
Parallel Ports.....	66
Appendix.....	69
Dimension	69
Special Features.....	70
J3: Feature Connector (J3: 44-pin 2.0mm IDC)	70

Chapter 1 Introducing the FB2642 System Board

Overview

The FB2642 is a Socket 370 all-in-one CPU card. This user's manual provides information on the physical features, installation, and BIOS setup of the FB2642.

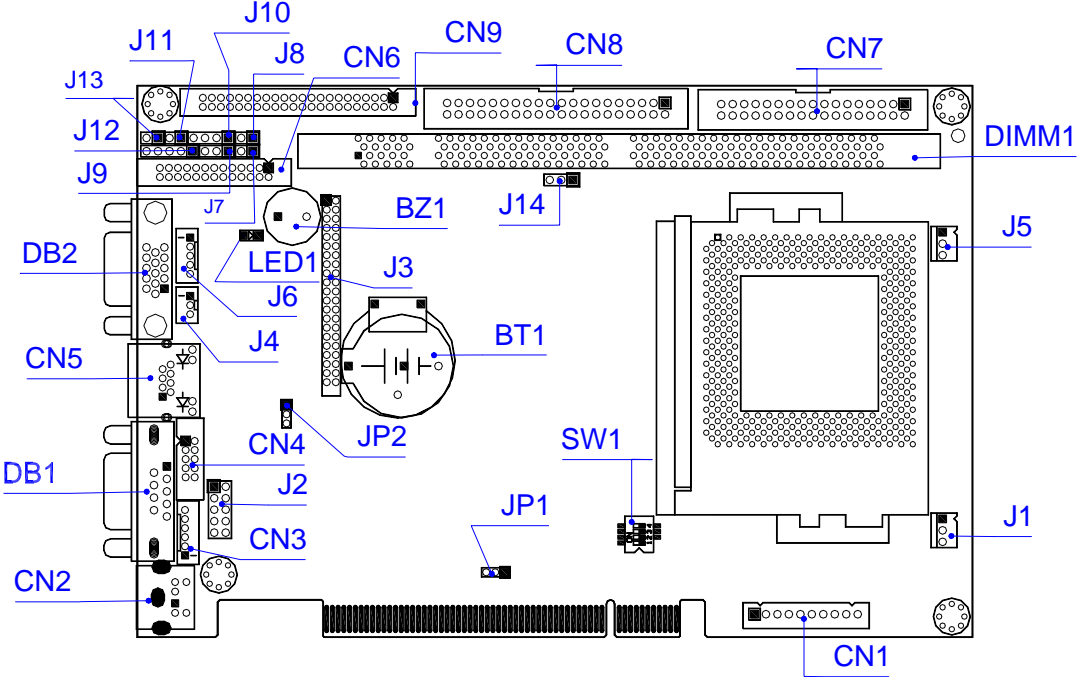
Built to unleash the total potential of the Pentium Processor, the FB2642 is a single boards computer capable of handling today's demanding requirements. Able to support up to 1.3 GHz / Pentium-III/Tualatin/Celeron/Coppermine CPUs, this unit supports 10/100M interface network port, synchronous pipe line burst SDRAM up to 512MB, and on board VGA port uses the 815E chipset with UMA share memory with 4MB caching buffer.

Each FB2642 has two ports for I/O communications. One RS-232C and one RS-232C / 422/485/IrDA ports are available. There is also a watchdog timer that can be configured from software to automatically reset the system or generate an interrupt. And for easy configuration, AMI BIOS are available.

Power management is also featured to lower the rate of consumption. The unit supports doze mode, <Suspend Mode> and <Standby mode> as well as it adheres to the "Green Function" standard.

The FB2642 is perfect for POS and POI applications, network systems, panel / MMI's, order entry kiosks and test equipment. The Compact size is only 185X122mm.

Layout



Specifications

- Supports 600MHz~1.300 GHz PIII/Tualatin/Celeron/Coppermine CPU. (Socket 370 with 0.18 and 0.13 micron technology)
- Compact size slot card with PICMG PCI expansion bus.
- Intel chipset 815E, ICH2 and 128KB or above L2 cache inside the CPUs.
- Supports one 168-pin DIMM socket (PC-100/133 SDRAM), 512MB maximum.
- 100M/10M Ethernet with RJ-45 connector.
- Intel 815E chipset provides CRT use UMA share memory VRAM with 4MB caching buffer.
- Parallel port, floppy and two IDE channels supports four IDE devices with ultra DMA 33. In addition, channel one IDE supports ultra DMA 33/66/100.
- One RS-232 and one RS-232/RS-422/RS-485/IrDA.
- PS/2 compatible keyboard and mouse interface.
- E2KEY function for safe CMOS data keeping. (Option)
- On-board buzzer and LED indicator.
- Flash BIOS with easy upgrade utility.
- Software programmable watchdog timer.
- Two USB ports and hardware monitoring functions.
- Provides CPU & case cooling fan connector for monitoring.
- Provide one piggyback space for panel link, audio and Intel LAN. (Optional)
- EMI Considered on every output signals.
- Compact size, 185 mm x 122 mm.

Packing List

Upon receiving the package, verify the following things. Should any of the mentioned happens, contact us for immediate service.

- Unpack and inspect the FB2642 package for possible damage that may occur during the delivery process.
- Verify the accessories in the package according to the packing list and see if there is anything missing or incorrect package is included.
- If the cable(s) you use to install the FB2642 is not supplied from us, please make sure the specification of the cable(s) is compatible with the FB2642 system board.

Note: after you install the FB2642, it is recommended that you keep the diskette or CD that contains drivers and document files, document copies, and unused cables in the carton for future use.

The following lists the accessories that may be included in your FB2642 package. Some accessories are optional items that are only shipped upon order.

- One FB2642 system board
- One compact disc containing manual file in PDF format and necessary drivers and utilities
- One 40-pin hard disk drive interface cable
- One 34-pin floppy drive interface cable
- One serial port and parallel port interface cable with bracket
- One mouse port adapter cable with bracket
- One 5-page hard copy of Quick Installation Guide
- One 2-port USB adapter cable (Optional)

Chapter 2 Hardware Installation

To set up a FB2642 system board, complete the description Chapter 2 and Chapter 3.

This chapter introduces the system board connectors, jumper settings and then guides you to apply them for field application.

Before Installation

Before you install the system board, make sure you follow the following descriptions.

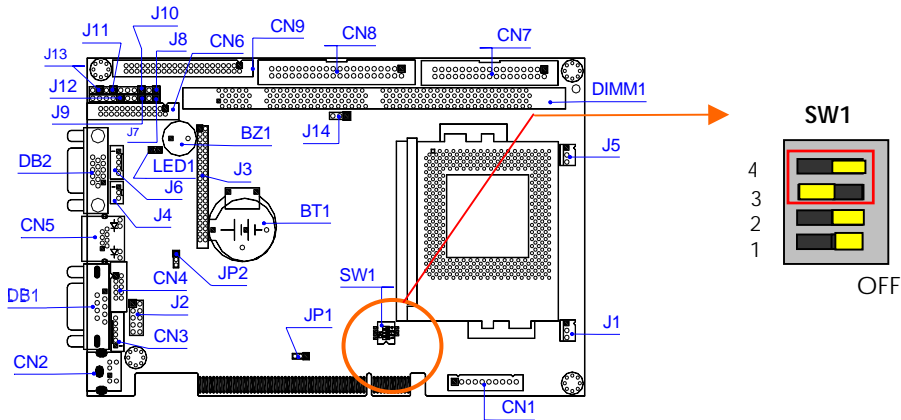
1. Before removing the board from its anti-static bag, wear an anti-static strap to prevent the generation of Electricity Static Discharge (ESD). The ESD may be created from human body that touches the board. It may do damage to the board circuit.
2. Install or unplug any connector, module, or add-on card, be sure that the power is disconnected from the system board. If not, this may damage the system board components, module, or the add-on-card.
3. Installing a heat sink and cooling fan is necessary for heat dissipation from your CPU. If heat sink or cooling fan is not mounted, this may cause the CPU fail due to over-heating problem.
4. When you connect the connectors and memory modules, be careful with the pin orientations.

Hardware Features

The following lists the connectors and jumpers to install the FB2642.

Item	Description
CN1	9-pin power connector
CN2, CN3	Keyboard and Mouse connector
CN4	10-pin RS-232 port 2 connector
CN5	RJ45-Lan connector
CN6	26-pin 2.0mm parallel port connector
CN7	34-pin 2.54mm floppy connector
CN8	40-pin 2.54mm IDE 1 hard disk connector
CN9	44-pin 2.0mm IDE 2 hard disk connector
J1, J5	3-pin for case/CPU cooling fan
J2	USB connector
J3	External Bus for Piggyback place with Lam, audio, Panel Link
J4	3-pin RS232C touch screen header for serial port 2
J6	5-pin for TTL I/O
J7	2-pin for external temperature sensor
J8	2-pin for external TX-LED with LAN
J9	3-pin for External power LED header
BZ1, J10	Onboard Buzzer and external speaker header
J11	2-pin HDD LED Indicator header
J12	5-pin RS232C IrDA header for serial port 2
J13	2-pin Reset header
JP1	To clear CMOS data
JP2	3-pin Terminal Resistor of Serial port 2
DB1	RS232 9-pin D - type male connector
DB2	CRT connector
LED1	Power LED indicator
SW1	To selects CPU base clock and RS232/RS422/RS485

□ **SW1 (3,4): Selecting CPU Base Clock and PCI Clock**

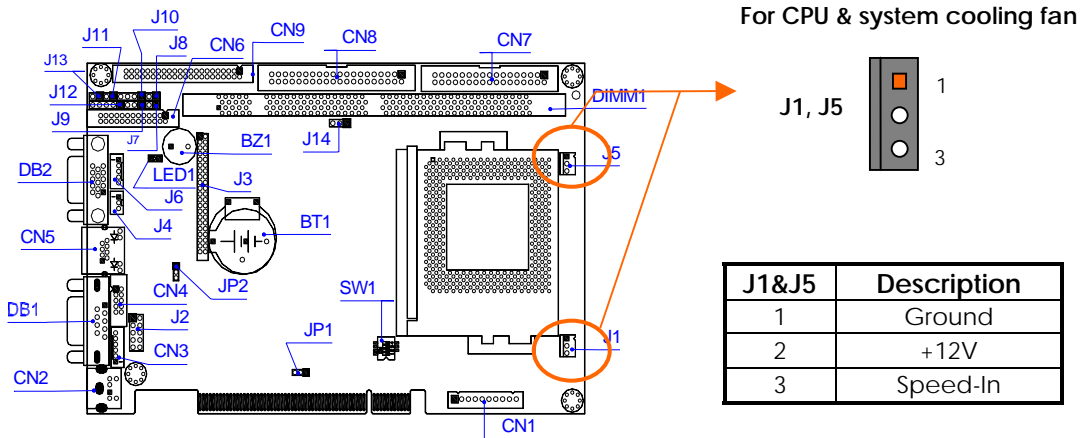


The following lists the switch settings of CPU Base Clock and PCI clock.

SW1-3	SW1-4	CPU Base Clock	PCI Clock	Remark
Off	Off	133 MHz	33 MHz	Tualatlin
Off	On	Reserved	Reserved	
On	Off	100Mhz	33Mhz	Default
On	On	66Mhz	33Mhz	

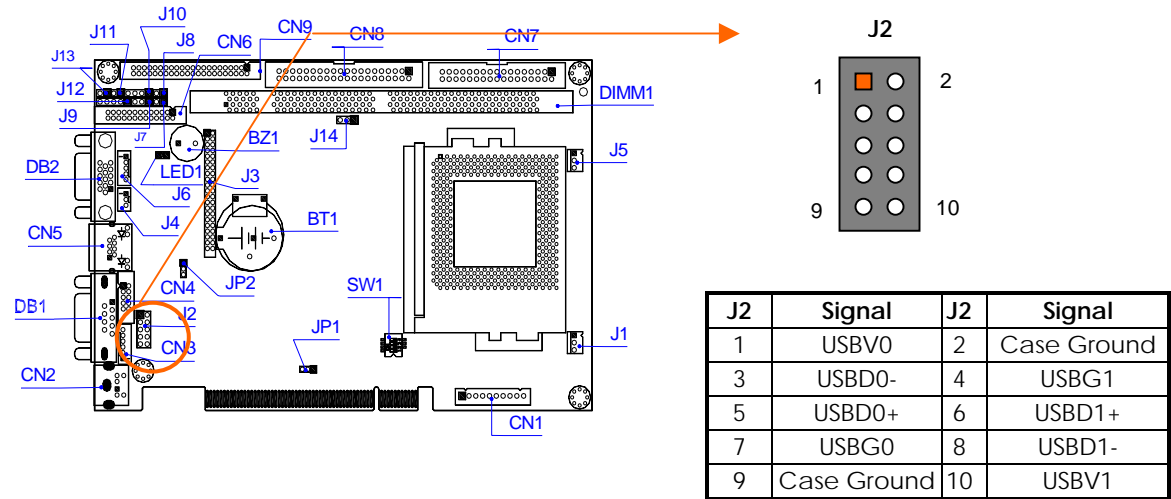
- ✧ Caution (*1): Avoid any of the following conditions that will directly destroy or severely cause damage to your CPU, or make your system unstable if you select an inappropriate base clock.
- ✧ Coppermine CPUs: Celeron over 66 MHz CPU base clock and PIII over 100/133 MHz CPU base clock
- ✧ Pentium III (Tualatlin) CPUs: Celeron over 100 MHz CPU base clock and PIII over 133 MHz CPU base clock

□ **J1 & J5: CPU Fan Connector & System Fan Connector**



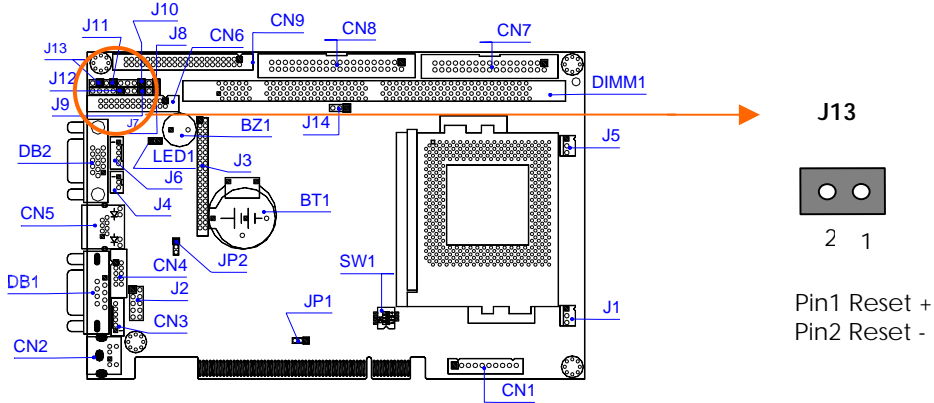
□ **J2: USB Connector**

J2 is a 10-pin connector. Use included adapter cable (Optional) for transferring to standard double port USB connector.

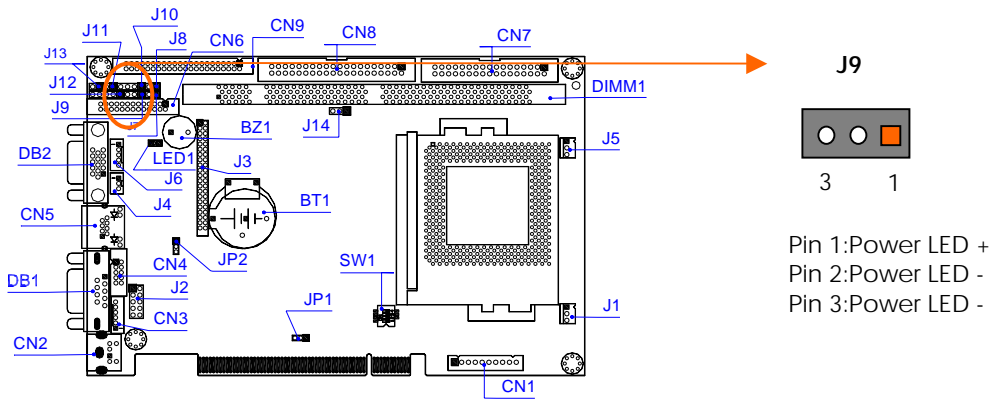


□ **J13: Reset Header**

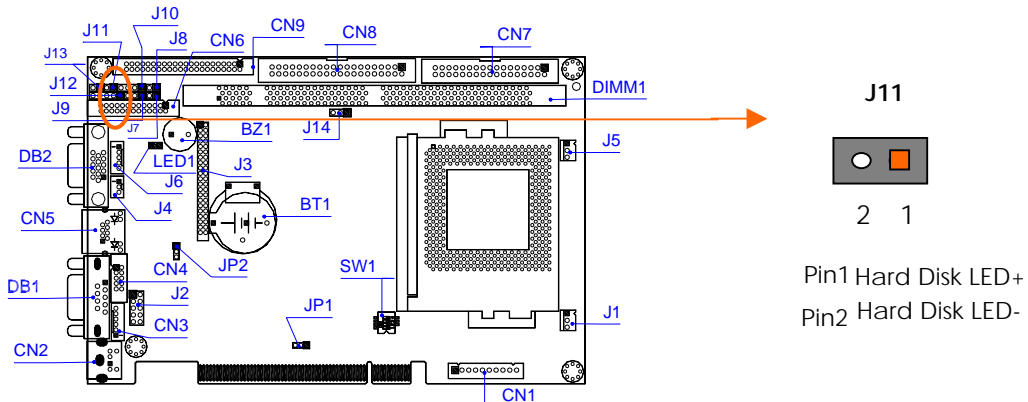
J13 is a 2-pin header for connecting to system reset bottom. Short-circuit these 2 pins to hardware reset FB2642 as well as restart system. It is similar to power off the system and then power it on again.



□ **J9: Power LED Header**

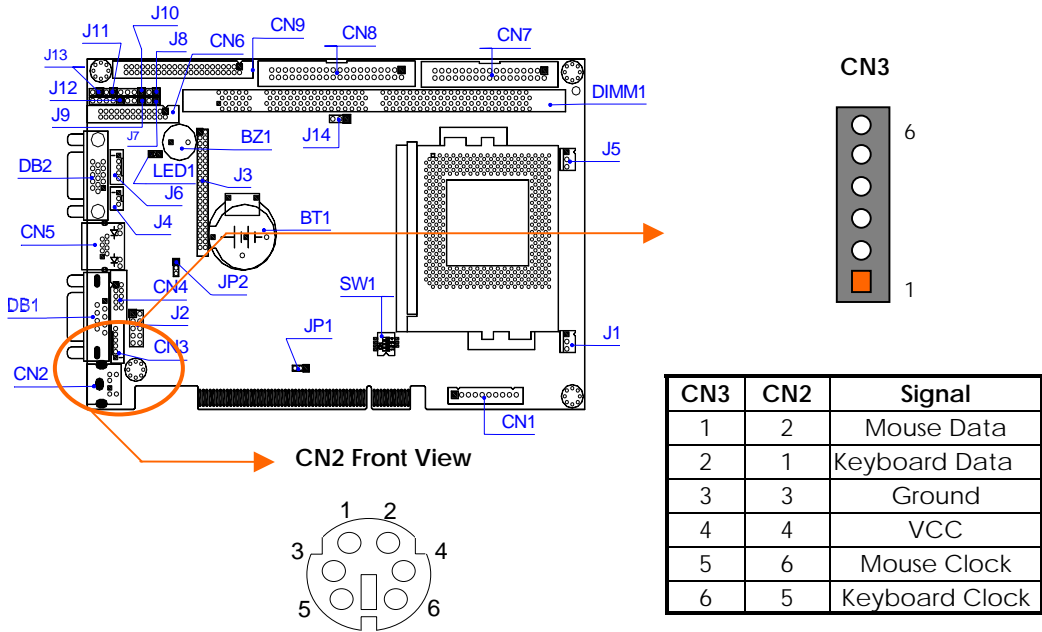


□ **J11: HDD LED Header**



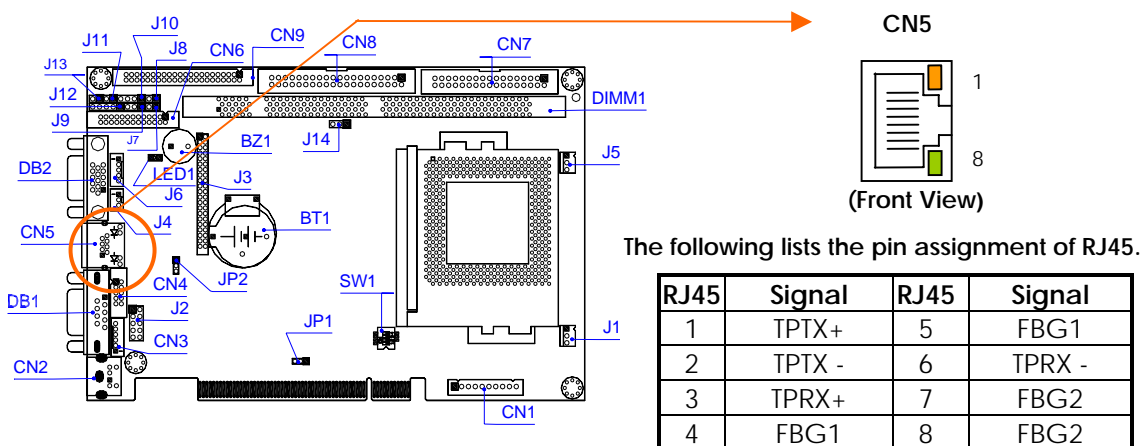
□ **CN2, CN3: Keyboard/Mouse Connector**

CN2 is a standard PS/2 type keyboard connector, so any PS/2 type keyboard can plug into CN2 directly without extra adapter cable. CN3 provides PS/2 mouse interface, use the included mouse adapter cable to connect between CN3 and standard PS/2 mouse.



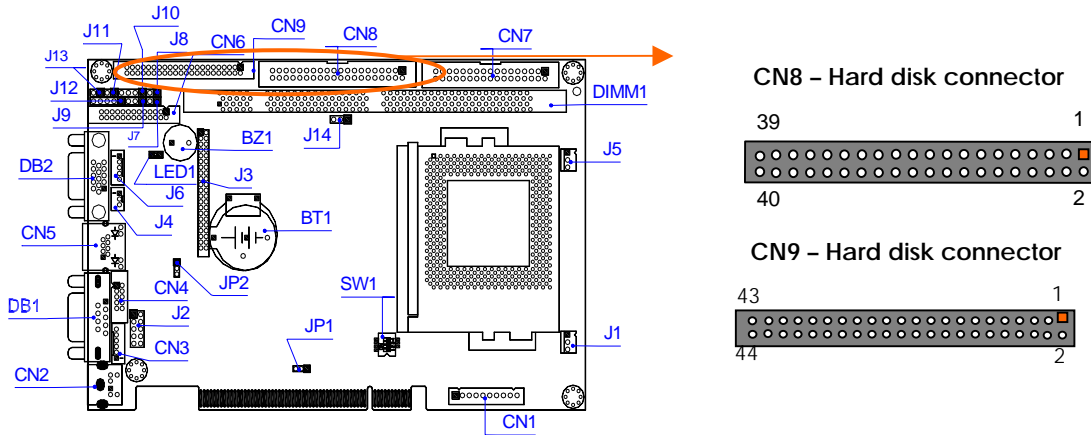
□ **CN5: RJ45 LAN Connector**

The CN5 contain LAN twist pair signals and LAN accesses indicator signal is RJ45 type connector with 2 LED indicators. The up side LED (orange) indicates data is accessing and the down side LED (green) indicates on-line status. (When lighted indicates on-line and off indicates off-line).



□ **CN8, CN9: IDE hard Disk Connector**

CN 8 is 40-pin 2.54mm IDE hard disk connector. CN9 is 44-pin 2.0mm IDC connectors. The included hard disk is able to attach up to four hard disk drives.

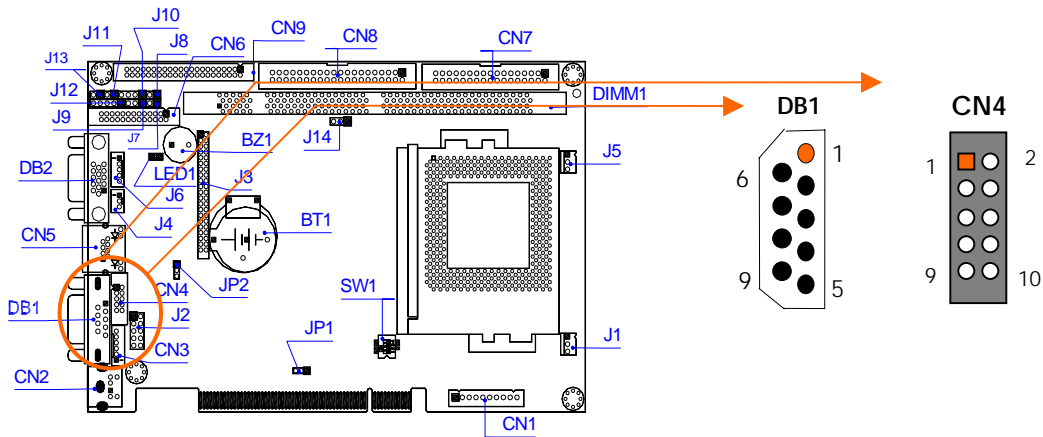


The following table lists the pin description of CN8, CN9.

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW	24	GROUND
25	-IOR	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AIN1	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41 (CN9)	VCC	42 (CN9)	VCC
43 (CN9)	GROUND	44 (CN9)	Not Used

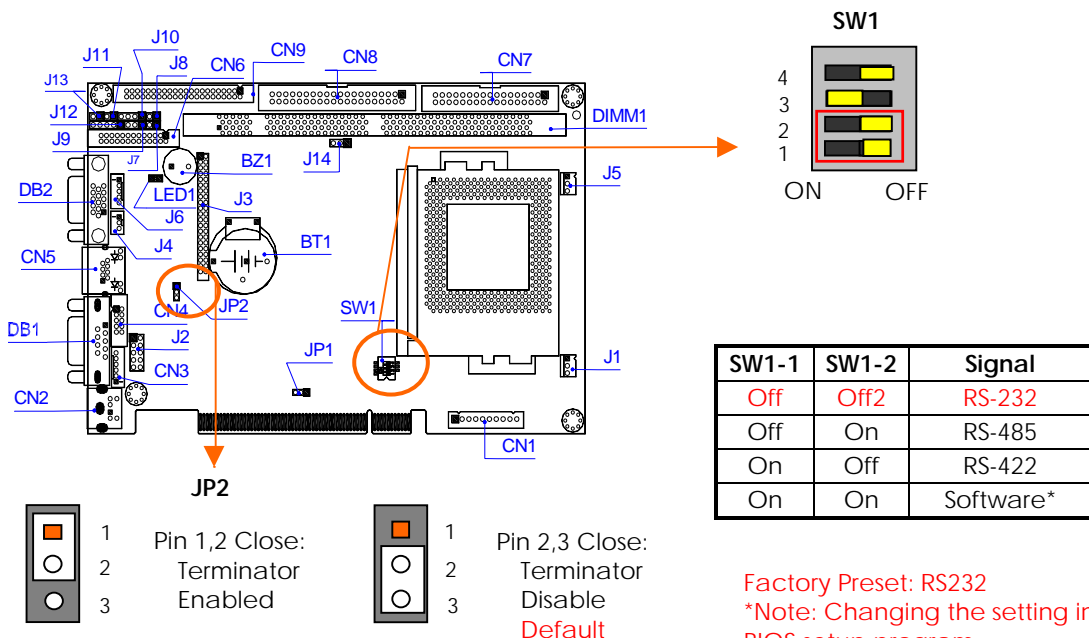
□ **DB1 & CN4: RS232 Serial Ports 1,2 Connectors and Jumpers**

The DB1 connector on bracket is 9-pin D-type male connector the serial port 2 adapter cables are used to transfer 10-pin IDC connector into standard DB9 connectors.



□ **Serial Port 2 (CN4, SW1, J12, J4, JP2)**

Serial port 2 is designed for multiple proposes. It could be RS-232C, RS-422 or RS-485 by selecting SW1 or changing the setting in BIOS setup program. And JP2 is use to enable or disable terminator if RS-485 mode is selected. Serial port 2 also could be configured as Infra (IrDA) interface by changing the setting in BIOS setup program. J12 is use to interface with Infra module. When touch screen module is used, you could connect J4 to touch screen controller directly and internally instead of connect from CN4 connector.

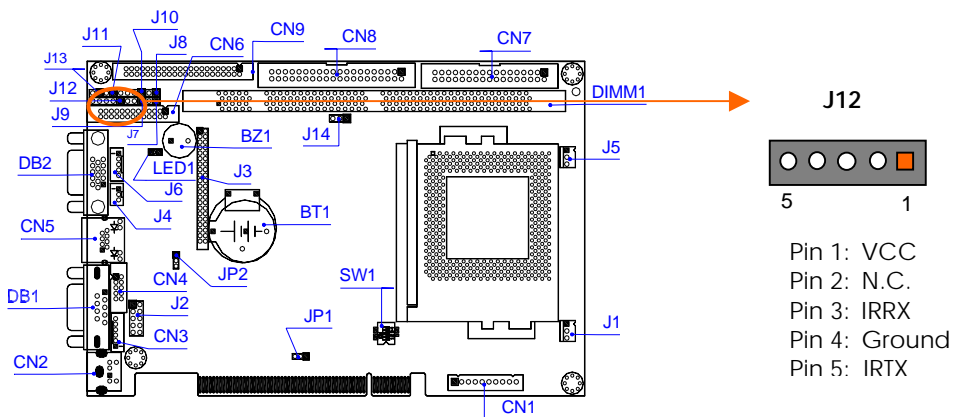


Factory Preset: RS232
*Note: Changing the setting in BIOS setup program

CN4	Signal	RS422	RS485	DB9
1	-DCD2			1
2	-DSR2			6
3	RXD2	RX-	485-	2
4	-RTS2	TX-		7
5	TXD2	RX+	485+	3
6	-CTS2	TX+		8
7	-DTR2			4
8	-RI2			9
9	GROUND			5
10	CASE GROUND			

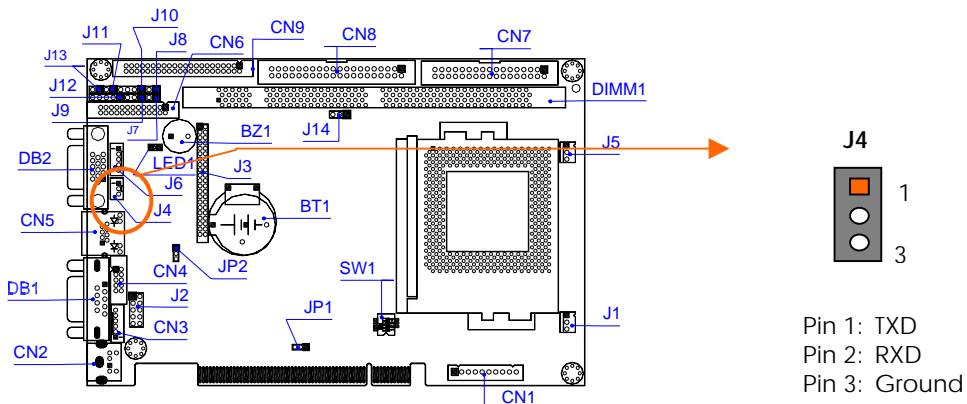
□ **J12: 5-pin Infrared Header**

J12 provides infrared signals of serial port 2. The infrared signal is used to interface with Infrared modules.



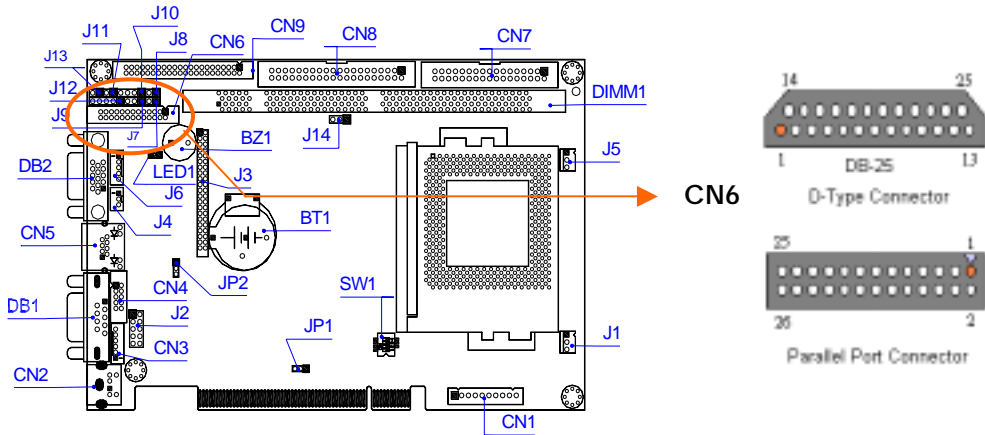
□ **J4: Touch Screen Header**

J4 provide basic RS-232C signals of serial port 2 respectively. The basic RS-232C signal is used to interface with touch screen controller internally.



□ **CN6: 26-pin Parallel Port Connector**

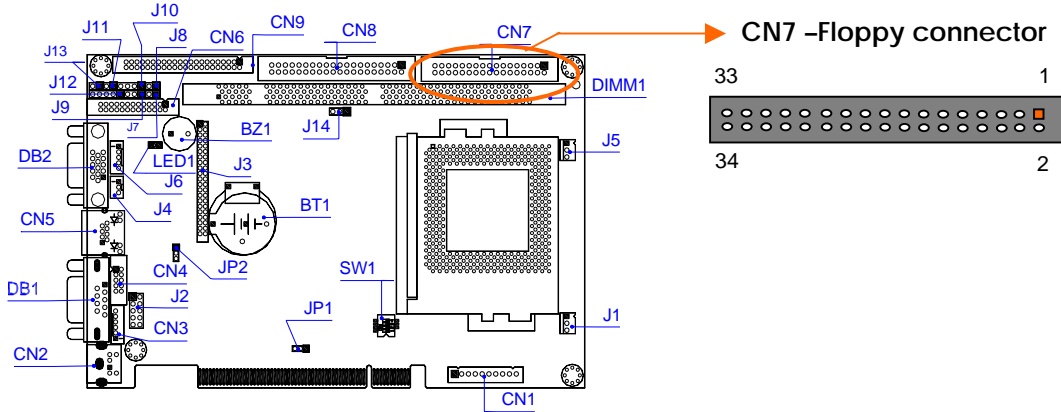
The included printer interface cable is used to transfer 26-pin connector into standard DB25 connector.



CN6	DB-25	Signal	CN6	DB-25	Signal
1	1	-STROBE	2	14	-AUTO FORM FEED
3	2	DATA 0	4	15	-ERROR
5	3	DATA 1	6	16	-INITIALIZE
7	4	DATA 2	8	17	-PRINTER SELECT IN
9	5	DATA 3	10	18	Ground
11	6	DATA 4	12	19	Ground
13	7	DATA 5	14	20	Ground
15	8	DATA 6	16	21	Ground
17	9	DATA 7	18	22	Ground
19	10	-ACKNOWLEDGE	20	23	Ground
21	11	BUSY	22	24	Ground
23	12	PAPER	24	25	Ground
25	13	PRINTER SELECT	26	--	No Used

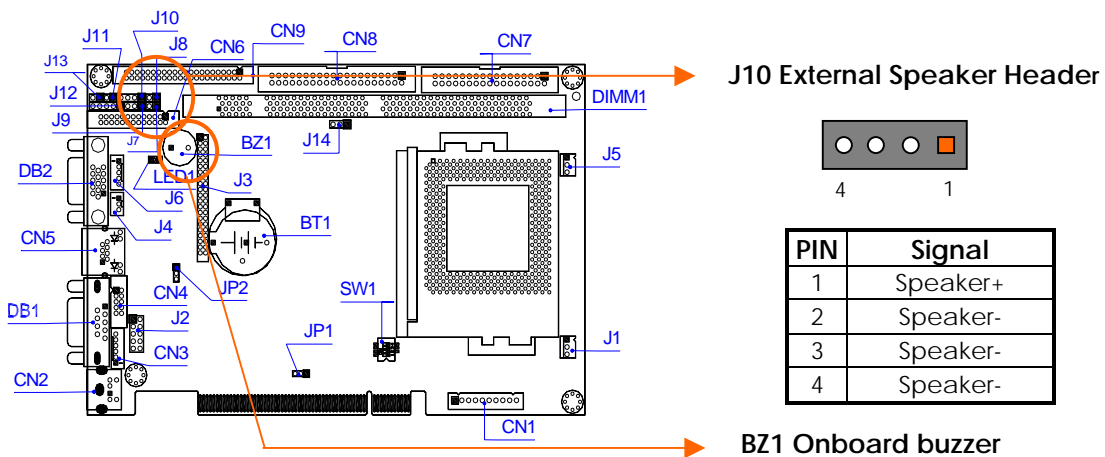
□ **CN7: Floppy Connector**

The included floppy drive interface cable is used standard 34-pin connector. The following table shows signal connections 34-pin connectors.



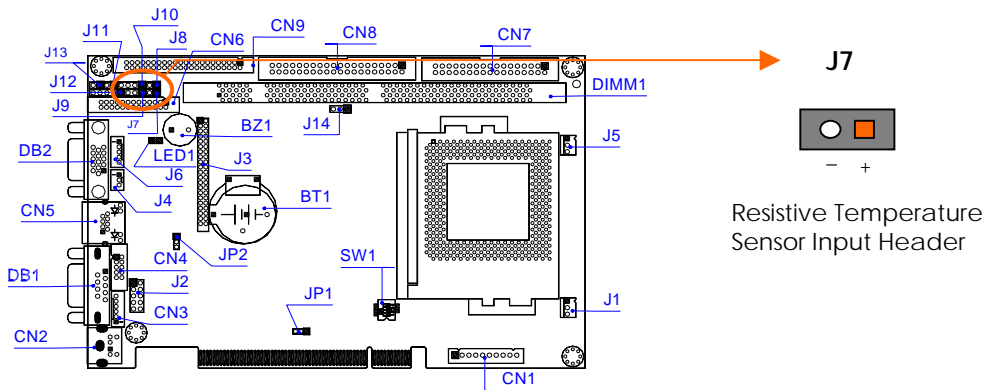
34-pin	Signal	34-pin	Signal
2	Drive Enable A	23	Ground
8	-Index	24	-Write Enable
12	-Select A	26	-Track 0
11	Ground	28	-Write Protect
16	-Motor A	29	Ground
14	- Select B	30	-Read Data
10	-Motor B	31	Ground
9	Ground	32	-Head
18	-Direction	33	NC
20	-Step	34	-Disk Change
22	-Write Data	Others	No Connection

□ **BZ1 & J10: On-Board Buzzer & External Speaker Header**



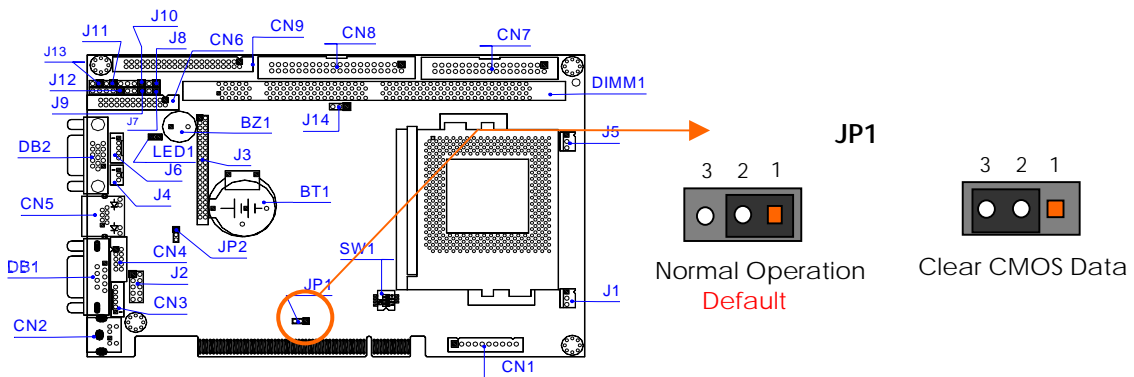
PIN	Signal
1	Speaker+
2	Speaker-
3	Speaker-
4	Speaker-

□ **J7: Temperature Sensor Header**



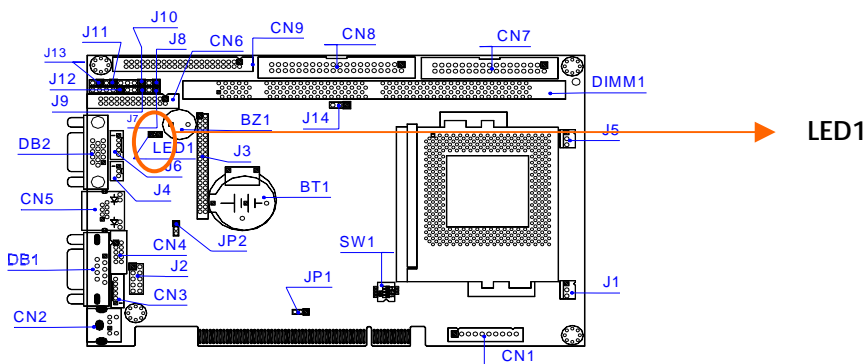
□ **JP1: CMOS Data Clear Jumper**

You can use JP1 to clear CMOS data. The CMOS store information like system date, time, boot up device, password, IRQ... that are set up with the BIOS. To clear the CMOS, set JP1 to 2-3 and then return to 1-2. The default setting is 1-2.

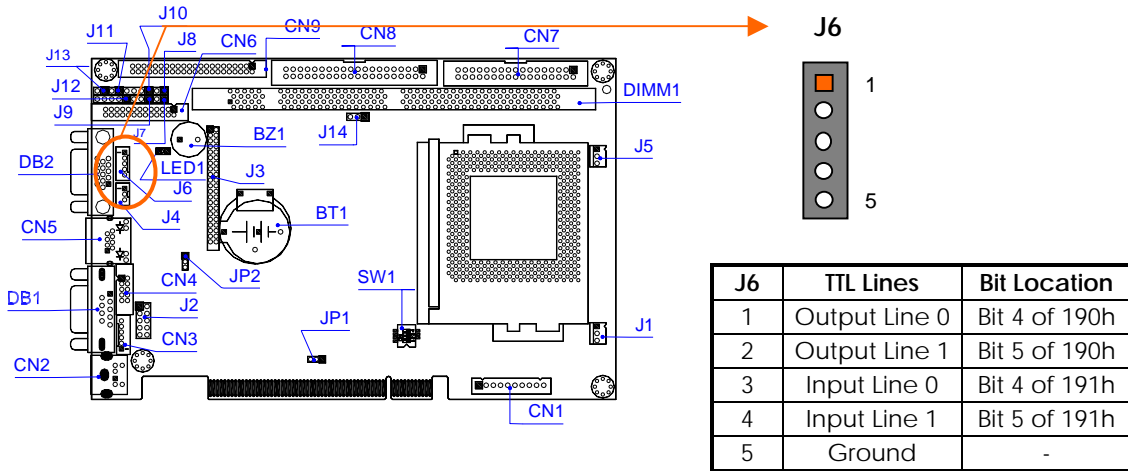


□ **LED1: On-Board Power LED**

LED1 indicates power is active when it lights.

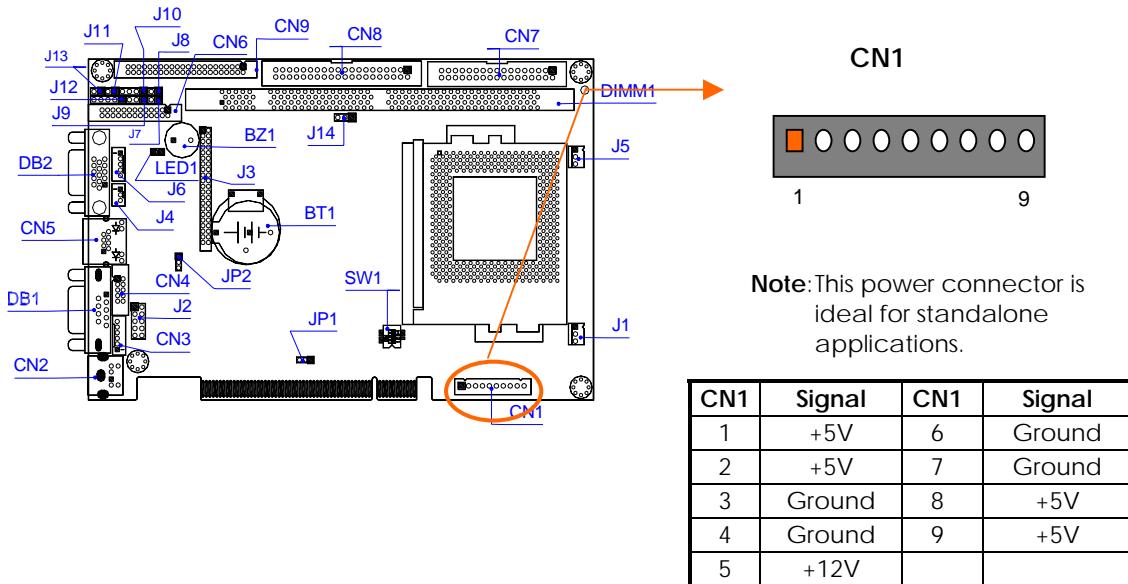


□ **J6: TTL I/O Connector**



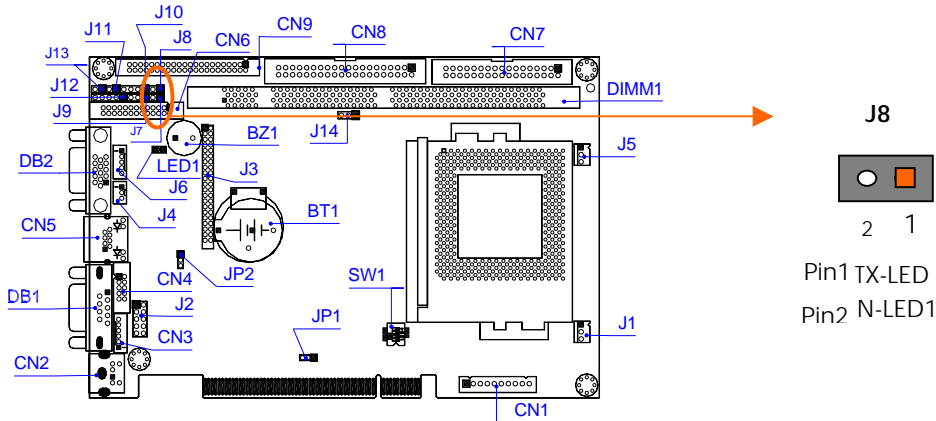
□ **CN1: Power Connector (9-pin 2.54mm JST)**

CN1 is the power connector for FB2642 is used with stand-alone applications.



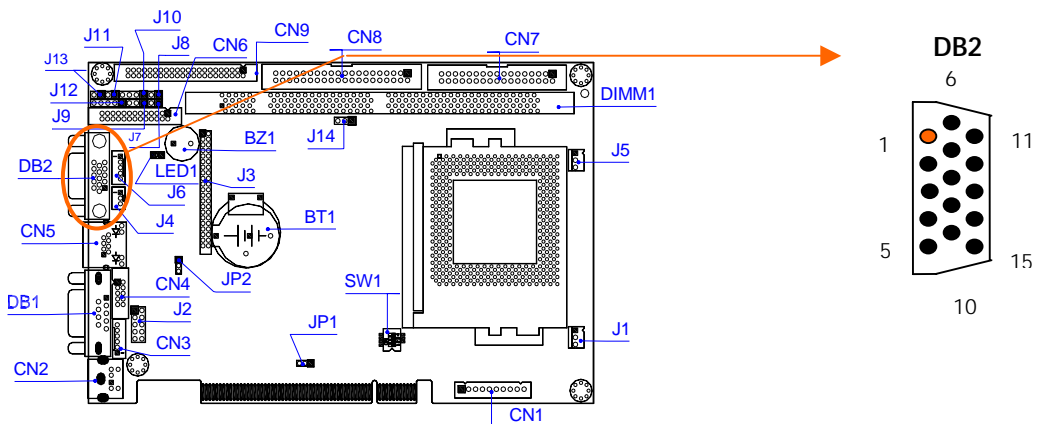
□ **J8: External TX-LED with LAN LED Header**

The J8 is LAN accesses indicator with LED indicators. The LED (FLASH) indicates data is accessing and LED (LIGHT) indicates on-line status. (When lighted indicates on-line and off indicates off-line).



□ **DB2: CRT connector**

The FB2642 supports a CRT colored monitor. It can be connected to create a compact video solution for the industrial environment. The VGA control in the 815E chipset and supports AGP, the VGA memory is UMA memory with 4MB caching buffer allows a maximum CRT resolution of 1280X1024 with 24bpp colors. The CRT is use to a standard CRT connector (DB2).



DB15	Signal	DB15	Signal
1	RED	Case	Case Ground
2	GREEN	5,10	Digital Ground
3	BLUE	6,7,8	Analog Ground
14	VSYNC	15	DDC Clock
13	HSYNC	12	DDC Data

Chapter 3 BIOS Setup

This chapter describes the BIOS setup.

Overview

BIOS are a program located on a Flash memory chip on a circuit board. It is used to initialize and set up the I/O peripherals and interface cards of the system, which includes time, date, hard disk drive, the ISA bus and connected devices such as the video display, diskette drive, and the keyboard. This program will not be lost when you turn off the system.

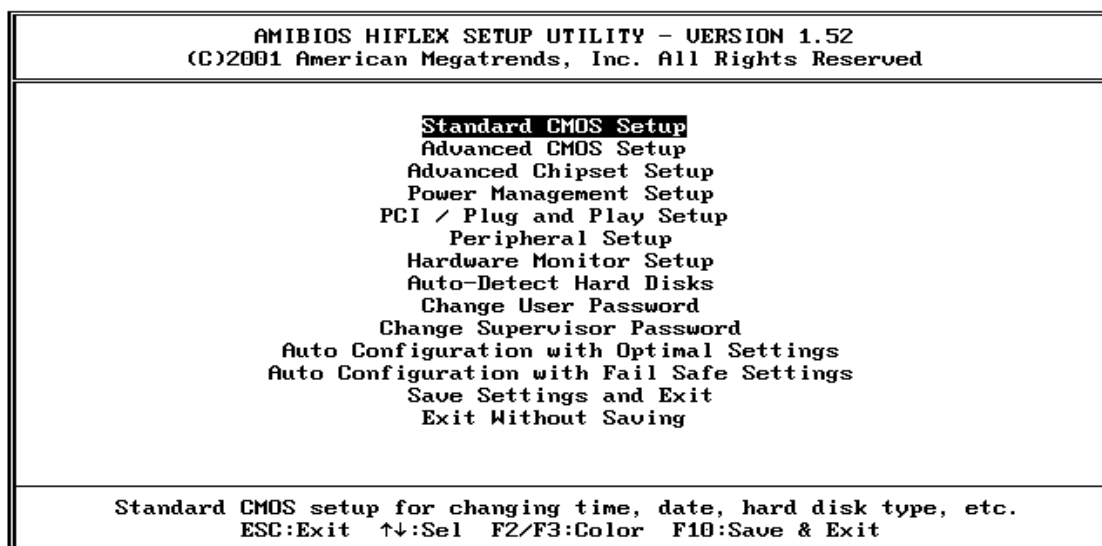
The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

All the changes you make will be saved in the system RAM and will not be lost after power-off.

When you start the system, the BIOS will perform a self-diagnostics test called Power On Self Test (POST) for all the attached devices, accessories, and the system. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

Note: Change the parameters when you fully understand their functions and subsequence.



BIOS Functions

On the menu, you can perform the following functions

1. Standard CMOS Setup
2. Advanced CMOS Setup
3. Advanced Chipset Setup
4. Power Management Setup
5. PCI/ Plug and Play Setup
6. Peripheral Setup
7. Hardware Monitor Setup
8. Auto-Detect Hard Disks
9. Change User Password
10. Change Supervisor Password
11. Auto Configuration with Optimal Settings: to auto configure the system according to optimal setting with pre-defined values. This is also the factory default setting of the system when you receive the board.
12. Auto Configuration with Fail Safe Settings: to configure the system in fail-safe mode with predefined values.
13. Save Settings and Exit: perform this function when you change the setting and exit the BIOS Setup program.
14. Exit without saving: perform this function when you want to exit the program and do not save the change.

Keyboard Convention

On the BIOS, the following keys can be used to operate and manage the menu:

Item	Function
ESC	To exit the current menu or message
Page Up/Page Down	To select a parameter
F1	To display the help menu if you do not know the purpose or function of the item you are going to configure
F2/F3	To change the color of the menu display. F2 is to go forward and F3 is to go backward.
UP/Down Arrow Keys	To go upward or downward to the desired item

STANDARD CMOS SETUP

This section describes basic system hardware configuration, system clock setup and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

AMIBIOS SETUP - STANDARD CMOS SETUP									
(C)2001 American Megatrends, Inc. All Rights Reserved									
Date (mm/dd/yyyy): Tue Dec 03, 2002					Base Memory: 0 KB				
Time (hh/mm/ss) : 08:33:02					Extd Memory: 0 MB				
Floppy Drive A:		1.44 MB 3½							
Floppy Drive B:		Not Installed							
	Type	Size	Cyln	Head	WPcom	Sec	LBA Mode	Blk Mode	PIO 32Bit Mode
Pri Master:	Auto								Off
Pri Slave:	Auto								Off
Sec Master:	Auto								Off
Sec Slave:	Auto								Off
Boot Sector Virus Protection					Disabled				
Month: Jan - Dec					ESC:Exit ↑↓:Sel				
Day: 01 - 31					PgUp/PgDn:Modify				
Year: 1980 - 2099					F1:Help F2/F3:Color				

□ Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

□ Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

□ Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks. For

the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

□ **Boot Sector Virus Protection**

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <*Disabled*>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

ADVANCED CMOS SETUP

AMIBIOS SETUP - ADVANCED CMOS SETUP		
(C)2001 American Megatrends, Inc. All Rights Reserved		
Quick Boot	Enabled	
1st Boot Device	IDE-0	
2nd Boot Device	Floppy	
3rd Boot Device	CD/DVD	
Try Other Boot Devices	Yes	
Initial Display Mode	BIOS	
Floppy Access Control	Read-Write	
Hard Disk Access Control	Read-Write	
S.M.A.R.T. for Hard Disks	Disabled	
BootUp Num-Lock	On	▲ Available Options:
Floppy Drive Swap	Disabled	Off
Floppy Drive Seek	Disabled	▶ On
PS/2 Mouse Support	Enabled	
System Keyboard	Absent	
Primary Display	Absent	
Password Check	Setup	
Boot To OS/2	No	
Wait For 'F1' If Error	Disabled	
Hit 'DEL' Message Display	Enabled	
L1 Cache	WriteBack	
L2 Cache	WriteBack	
C000, 16k Shadow	Cached/WP	
C400, 16k Shadow	Cached/WP	
C800, 16k Shadow	Cached/WP	
CC00, 16k Shadow	Disabled	
D000, 16k Shadow	Disabled	
D400, 16k Shadow	Disabled	
D800, 16k Shadow	Disabled	
DC00, 16k Shadow	Disabled	

ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

This section describes the configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

❑ Quick Boot

This field is used to activate the quick boot function of the system. When set to Enabled,

1. BIOS will not wait for up to 40 seconds if a Ready signal is not received from the IDE drive, and will not configure its drive.
2. BIOS will not wait for 0.5 seconds after sending a RESET signal to the IDE drive.
3. You cannot run BIOS Setup at system boot since there is no delay for the Hit, Del. To run Setup message.

Available Options: Disabled, Enabled

Default setting: Enabled

1st –3rd Boot Device

These fields determine where the system attempts to look for the boot drive priority for an operating system. The default procedure is to check the hard disk, and then the floppy drive, and last the CDROM.

Available options: Disabled, IDE0-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CD/DVD, USB-FLOPPY, USB-CDROM, USB-HDD and SCSI, Network

Default setting: IDE-0 for 1st Boot device; Floppy for 2nd Boot Device; CDROM for 3rd Boot Device

Try Other Boot Device

If all 3 1st –3rd boot devices specified by CMOS setup are not available to boot, BIOS will try to boot other available devices in following order if this question is set to "Enabled".

Initial Display Mode

This field specifies can set Normal POST screen (BIOS) or Boot with logo, no POST messages (Client).

Floppy Access Control

This field specifies the read/write access when booting from a floppy drive.

Available options: Normal, Read-only

Default setting: Normal

Hard Disk Access Control

This field specifies the read/write access when booting from a HDD drive.

Available options: Normal, Read-only

Default setting: Normal

S.M.A.R.T for Hard Disk

This field is used to activate the S.M.A.R.T (System Management and Reporting Technologies) function for S.M.A.R.T HDD drives. This function requires an application that can give S.M.A.R.T message.

Available options: Disabled, Enabled

Default: Disabled

Boot Up Num-lock

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Available options: On, Off

Default setting: On

Floppy Drive Swap

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of **Disabled** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is **<Enabled>**, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Available options: Disabled, Enabled

Default setting: Disabled

Floppy Drive Seek

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.

Available Options: Disabled, Enabled

Default setting: Disabled

PS/2 Mouse Support

The setting of **Enabled** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. **Disabled** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Available options: Disabled, Enabled

Default setting: Enable

System Keyboard

This field specifies if an error message should be prompted when a keyboard is not attached.

Available options: Absent, Present

Default setting: Absent

Primary Display

The field specifies the type of monitor installed in the system.

Available options: Absent, VGA/EGA, CGA40x25, CGA80x25, and Mono

Default setting: Absent

Password Check

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If **Always** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If **Setup** is chosen, the password prompt appears if the BIOS executed.

Available options: Setup, Always

Default setting: Setup

Boot To OS2

If OS2 operating system is used, and the system RAM is over 64MB, please select yes. Otherwise, select No.

Available options: Yes, No

Default setting: No

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this field is set to **Disabled**, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Available options: Disabled, Enabled

Default setting: Disabled

Hit 'DEL' Message Display

Set this field to **Disabled** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available options: Disabled, Enabled

Default setting: Enabled

□ **C000, 32k Shadow - E800, 32k shadow**

These fields control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
2. **Enabled:** The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
3. **Cached/WP:** The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Available options: Disabled, Enabled, Cached

Default setting: Disabled

Default setting: Disable

ADVANCED CHIPSET SETUP

This section describes the configuration of the board's chipset features.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
SDRAM Timing by SPD	Disabled	Available Options:
DRAM Refresh	15.6/11.7 uS	▶ Disabled
DRAM Cycle time (SCLKs)	7/9	Enabled
CAS# Latency (SCLKs)	3	
RAS to CAS delay (SCLKs)	3	
SDRAM RAS# Precharge (SCLKs)	3	
Internal Graphics Mode Select	1MB	
AGP Aperture Window	64MB	
CPU Latency Timer	Disabled	
USB Function	Enabled	
USB Device Legacy Support	All Device	
		ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

❑ SDRAM Timing by SPD

SPD represents Serial Presence Detect. It is an 8-bit, 2048 bits EEPROM, built on the SDRAM for 100 MHz frequencies. If the installed SDRAM supports SPD function, select SPD. If not, you can select based on other access time of the SDRAM.

Available Options: Disabled, Enabled

Default setting: Disabled

❑ DRAM Refresh

This specifies the DRAM refresh rate.

Available Options: 15.6/11.7 us, 7.8/5.85 us and 1.28/0.96 us

Default setting: 15.6/11.7 us

❑ DRAM Cycle Time (SCLKs)

This field specifies control the number of DRAM for an access cycles.

Available Options: 5/7 and 7/9

Default setting: 7/9

CAS# Latency (SCLKs)

This field specifies the latency for the Synchronous DRAM system memory signals.

Available Options: 3, 2

Default setting: 3

RAS# to CAS# delay (SCLKs)

This field specifies the length of the delay inserted between RAS and CAS signals of the Synchronous DRAM system access cycle when SDRAM is installed.

Available Options: 3, 2

Default setting: 3

SDRAM RAS# Precharge (SCLKs)

This field specifies the length of the RAS precharge part of the Synchronous DRAM access cycle when SDRAM is installed.

Available Options: 3, 2

Default setting: 3

Internal Graphics Mode Select

This field Enable/Disable the internal graphics device and selects the amount of main memory that is dedicated to support the internal graphics device in VGA (non-linear) mode only.

Available Options: 512kB, 1MB and Disable

Default setting: 1 MB

Graphics Aperture Size

This field specifies the system memory size that can be used by the Accelerated Graphics Port (AGP).

Available Options: 32MB, 64MB

Default setting: 64 MB

CPU Latency Timer

This field specifies the latency for the Synchronous DRAM system memory signals.

Available Options: 3, 2

Default setting: 3

USB Function

Select Enabled if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Enabled

Default setting: Enabled

USB Device Legacy Support

Select All Device if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Mice and All Devices

Default setting: All Devices

POWER MANAGEMENT

AMIBIOS SETUP - POWER MANAGEMENT SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
Power Management/APM	Enabled	Available Options:
Video Power Down Mode	Disabled	Disabled
Hard Disk Power Down Mode	Disabled	▶ Enabled
Standby Time Out	Disabled	
Suspend Time Out	Disabled	
		ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

Power Management /APM

Select Enabled to activate the chipset Power Management and APM (Advanced Power Management) features.

Available Options: Disabled, Enabled

Default setting: Enabled

Video Power Down Mode

This field specifies the power conserving state that video subsystem enters after the specified period of display inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

Hard Disk Power Down Mode

This field specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

□ **Standby Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in full power on state. When this length of time expires, the system enters Standby power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute

Default setting: Disabled

□ **Suspend Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in Standby state. When this length of time expires, the system enters Suspend power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

PCI/PLUG AND PLAY

AMIBIOS SETUP - PCI / PLUG AND PLAY SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	No	Available Options: ▶ No Yes
Clear NVRAM on Every Boot	No	
PCI Latency Timer (PCI Clocks)	64	
Primary Graphics Adapter	Auto	
Allocate IRQ to PCI UGA	No	
PCI IDE BusMaster	Disabled	
DMA Channel 0	PnP	
DMA Channel 1	PnP	
DMA Channel 3	PnP	
DMA Channel 5	PnP	
DMA Channel 6	PnP	
DMA Channel 7	PnP	
IRQ3	PCI/PnP	
IRQ4	PCI/PnP	
IRQ5	PCI/PnP	
IRQ7	PCI/PnP	
IRQ9	PCI/PnP	
IRQ11	PCI/PnP	
IRQ14	PCI/PnP	
IRQ15	PCI/PnP	
		ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

Plug and Plug Aware O/S

Set to Yes to inform BIOS that the operating system can handle Plug and Play (PnP) devices.

Available Options: Yes, No

Default setting: No

PCI Latency Timer

This field specifies the latency timings (in PCI clock) PCI devices installed in the PCI expansion bus.

Available Options: 32, 64, 96, 128, 160,192, 224, and 248

Default setting: 64

Primary Graphics Adapter

This field specifies which VGA display will be used when the system is boot. You can select either the onboard AGP or the VGA card installed on the PCI bus.

Available Options: AGP, PCI

Default setting: PCI

PCI VGA Palette Snoop

When Enabled is selected, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit. (0 is disabled).

Available Options:

Disabled: Data read and written by the CPU is only directed to the PCI VGA devices palette registers.

Enabled: Data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device palette registers, permitting the palette registers of both devices to be identical.

Default setting: Disable

Allocate IRQ to PCI AGP

When a PCI or AGP VGA device is installed, you can assign an IRQ to this device. Selecting Yes, BIOS will auto-assign IRQ to the device. Selecting No, no IRQ will be assigned to the VGA device.

Available Options: Yes, No

Default setting: No

PCI IDE BusMaster

This option is to specify that the IDE controller on the PCI local bus have bus-mastering capability.

Available Options: Enable, Disable

Default setting: Disable

DMA Channel 0 – 7

When I/O resources are controlled manually, you can assign each system DMA as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

Available Options: PnP, ISA/EISA

Default setting: PnP

□ **IRQ 3 –15**

When I/O resources are controlled manually, you can assign each system interrupt as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

PERIPHERAL SETUP

This section describes the function of peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP (C)2001 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Auto	Available Options: ▶ Auto Disabled Enabled ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color
OnBoard Serial Port1	Auto	
OnBoard Serial Port2	Auto	
OnBoard Parallel Port	Auto	
Parallel Port Mode	Normal	
Parallel Port IRQ	Auto	
Parallel Port DMA Channel	N/A	
Read Com Port Mode of Status	Hardware	
Com Port Mode Selection	RS-232	
On-Chip IDE	Both	

❑ OnBoard FDC

This field enables the floppy drive controller on the FB2642.

Available Options: Disabled, Enabled and Auto

Default setting: Auto

❑ OnBoard Serial Port 1

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: Auto

❑ OnBoard Serial Port 2

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: Auto

OnBoard Parallel Port

This field selects the I/O port address for parallel port.

Available Options: Auto, Disabled, 378, 278, and 3BCH

Default setting: Auto

Parallel Port Mode

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

Available Options: N/A, Normal, Bi-Dir, EPP, and ECP

Default setting: Normal

Parallel Port IRQ

This field specifies the IRQ for the parallel port.

Available Options: Auto, N/A, 5, 7

Default setting: Auto

Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

Available Options: N/A, 0,1,3

Default setting: N/A

Read Com Port Mode State

These fields are auto detected SW1-4 Setting, that can set use BIOS or adjust SW1.

Available Options: Software, Hardware

Default setting: Hardware

Com Port Mode Selection

These fields item can select RS-232, RS-422, and RS-485 of Serial port 2.

Available Options: RS-232, RS-422 and RS-485

Default setting: RS-232

□ **On-Chip IDE**

This field specifies the IDE channel that can be applied when using CN3 IDE hard disk connector.

Available Options: Disabled, Primary, and Secondary, Both

Default setting: Both

Hardware Monitor Setup

On the Hardware Monitor Setup screen, you can set up or monitor the system temperature, CPU voltage, and CPU fan speed...

AMIBIOS SETUP - HARDWARE MONITOR SETUP (C)2001 American Megatrends, Inc. All Rights Reserved	
Current CPU Temperature	0°C/32°F
Current System Temperature	0°C/32°F
Current Ext. Temperature	0°C/32°F
Fan1 Speed	0 RPM
Fan2 Speed	0 RPM
CPU1 VCORE	+1.793U
CPU2 VCORE	+1.499U
+ 1.800U	+1.798U
+ 2.500U	+2.494U
+ 3.300U	+3.284U
+ 5.000U	+4.977U
+ 12.00U	+11.997U
- 12.00U	-12.420U
VBAT	+3.284U
ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color	

❑ System Hardware Monitor

In this field, you can monitor or detect the followings items. These items are view-only and cannot be changed.

- Current CPU Temperature
- Current System Temperature
- Current Ext. Temperature
- Fan1 Speed
- Fan2 Speed
- CPU1 VCORE
- CPU2 VCORE
- +1.800V
- +2.500V
- +3.300V
- +5.000V
- +12.00V
- -12.00V
- VBAT (On board Battery)

Password Setup

There are two security passwords: Supervisor and User. Supervisor is a privileged person that can change the User password from the BIOS.

According to the default setting, both access passwords are not set up and are only valid after you set the password from the BIOS.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Type the desired password (up to 8 character length) when you see the message, "Enter New Supervisor Password."
3. Then you can go on to set a user password (up to 8 character length) if required. Note that you cannot configure the User password until the Supervisor password is set up.
4. Enter Advanced CMOS Setup screen and point to the Password Checkup field.
5. Select Always or Setup.
 - ✧ **Always:** a visitor who attempts to enter BIOS or operating system will be prompted for password.
 - ✧ **Setup:** a visitor who attempts to the operating system will be prompted for user password. You can enter either User password or Supervisor password.
6. Point to **Save Settings and Exit** and press Enter.
7. Press Y when you see the message, "Save Current Settings and Exit (Y/N)?"

Note: it is suggested that you write down the password in a safe place to avoid that password may be forgotten or missing.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Press Enter instead of entering any character when you see the message, "Enter New Supervisor Password."
3. Thus you can disable the password.

Chapter 4 Driver and Utility

The enclosed diskette includes FB2642 VGA driver and LAN driver.

VGA Driver for WIN98/WIN95

Step 1: To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>VGA>I815e>WIN98. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.

Step 2: Execute WIN9Xe67.exe file.

Step 3: The screen shows the SETUP type. Press any key to enter the main menu.

Step 4: As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

Step 5: In the WINDOWS98/ME, you can find the <DISPLAYL> icon located in the {CONTROL PANEL} group.

Step 6: Adjust the <Refresh Rate>, and <Resolution>.

Note: In the VGA>INTEL>I815e NT4.0, 2000 or XP directory, a Readme_xxx.txt file is included to provide installation information or Visit to <http://developer.intel.com/design/software/drivers/platform/inf.htm>

BIOS Flash Utility

In the <UTILITY> directory, there is the FLASH835.EXE file.

Step 1: Use the FLASH835.EXE program to update the BIOS setting.

Step 2: And then refer to the chapter "BIOS Setup", as the steps to modify BIOS.

Step 3: Now the CPU board's BIOS loaded with is the newest program; user can use it to modify BIOS function in the future, when the BIOS add some functions.

LAN Utility

Step 1: To install the LAN utility OR driver, insert the CD ROM into the CD ROM device, and enter DRIVER>LAN>RTL8139C>DIAG. If your system is not equipped with a CD ROM device, copy the LAN VGA driver from the CD ROM to a 1.44" diskette.

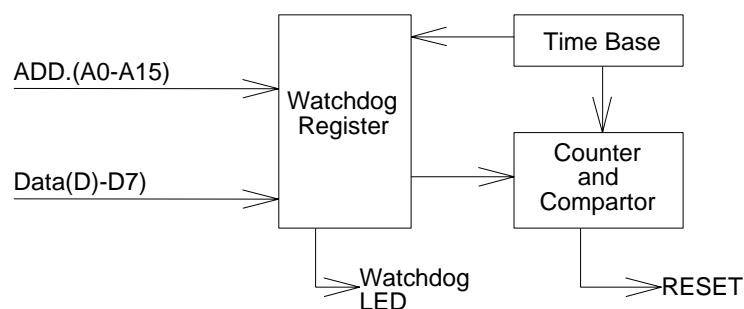
Step 2 Execute install.exe file.

Note: In the LAN directory, a HELPME.EXE file is included to provide installation information

Watchdog Timer

This section describes how to use the Watchdog Timer, including disabled, enabled, and trigger functions.

The FB2642 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be set from 1 to 255 seconds or minutes.



The CD-ROM includes a Watch Dog demo file. In the file, there are 3 execution programs written in different forms. The sub-directories of the file are:

1. WATCHDOG/ASSEMBLE: Library and Test Program written in Assembly Language
2. WATCHDOG/TURBOC: Library and Test Program written in Turbo C++

The WATCHDOG includes a demonstration program established for users who would like to configure the Watchdog timer by themselves.

Note: In the WATCHDOG directory, README.TXT file is included to provide demo program information.

Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect system crashes or hang-ups. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, it will be set to non-zero value to watchdog counter and start to count down again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.

The factor of the watchdog timer time-out constant is approximately 1 seconds. The period for the watchdog timer time-out is between 1 to FF timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Time Factor	Time-Out Period (Seconds)	Time-Out Period (Minutes)
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
"	"	"
"	"	"
"	"	"
FF	FF	FF

Watchdog Timer Enable & Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in the next trigger. Below is a Turbo C++ program, which demonstrates how to trigger the watchdog timer:

```
#include "stdio.H"
#include "WDLIB.H"

main()
{
char WD_TIME=0x6;

InitWD(equWdUnitS);
printf ("Enable watchdog");
//Trigger watchdog Timer Output is 6 seconds
EnWD(WD_TIME);
}
```

Watchdog Timer Disabled

To disable the watchdog timer, simply write DisWD() function.

```
#include "stdio.H"
#include "WDLIB.H"

main()
{
  InitWD(equWdUnitS);
  printf ("Disable Watch Dog");
  //Disable watch dog
  DisWD();
}
```

Programming RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 precedes the transmission, which needs control the TXC signal, and the installing, steps are as follows:

- Step 1: Enable TXC
- Step 2: Send out data
- Step 3: Waiting for data empty
- Step 4: Disable TXC

Note: Please refer to the section of the "Serial Ports" in the Chapter "Technical Reference" for the detail description of the COM port's register.

□ **Initialize COM port**

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the FB2642 CPU card's DTR signal to the RS-485 's TXC communication.

□ **Send out one character (Transmit)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

□ **Send out one block data (Transmit – the data more than two characters)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

❑ **Receive data**

The RS-485's operation of receiving data is in the same of the RS-232's.

❑ **Basic Language Example**

a. Initial 86C450 UART

```
10 OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20 REM Reset DTR
30 OUT &H3FC, (INP(%H3FC) AND &HFA)
40 RETURN
```

b. Send out one character to COM1

```
10 REM Enable transmitter by setting DTR ON
20 OUT &H3FC, (INP(&H3FC) OR &H01)
30 REM Send out one character
40 PRINT #1, OUTCHR$
50 REM Check transmitter holding register and shift register
60 IF ((INP(&H3FD) AND &H60) >0) THEN 60
70 REM Disable transmitter by resetting DTR
80 OUT &H3FC, (INP(&H3FC) AND &HEF)
90 RETURN
```

❑ **c. Receive one character from COM1**

```
10 REM Check COM1: receiver buffer
20 IF LOF(1)<256 THEN 70
30 REM Receiver buffer is empty
40 INPSTR$"
```



```
50    RETURN
60    REM Read one character from COM1: buffer
70    INPSTR$=INPUT$(1,#1)
80    RETURN
```

NOTE: The example of the above program is based on COM1 (I/O Address 3F8h).
The RS-422/RS-485 of the FB2642 uses COM2. If you want to program it, please refer to the BIOS Setup for COM2 address setup.

Chapter 5 Technical Reference

This section outlines the errors that may occur when you operate the system, and also gives you the suggestions on solving the problems.

Topic include:

- Trouble Shooting for Error Messages
- Technical Reference

Trouble Shooting for Error Messages

The following information informs the error messages and troubleshooting. Please adjust your systems according to the messages below. Make sure all the components and connectors are in proper position and firmly attached. If the errors still exist, please contact with your distributor for maintenance.

❑ POST BEEP

Currently there are two kinds of beep codes in BIOS setup.

- One indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by three short beeps.
- The other indicates that an error has occurred in your DRAM. This beep code consists of a constant single long beep.

❑ CMOS BATTERY FAILURE

When the CMOS battery is out of work or has run out, the user has to replace it with a new battery.

❑ **CMOS CHECKSUM ERROR**

This error informs that the CMOS has corrupted. When the battery runs weak, this situation might happen. Please check the battery and change a new one when necessary.

❑ **DISPLAY SWITCH IS SET INCORRECTLY**

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in BIOS Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter BIOS Setup and change the video selection.

❑ **DISK BOOT FAILURE**

When you can't find the boot device, insert a system disk into Drive A and press < Enter >. Make sure both the controller and cables are all in proper positions, and also make sure the disk is formatted. Then reboot the system.

❑ **DISKETTE DRIVES OR TYPES MISMATCH ERROR**

When the diskette drive type is different from CMOS, please run setup or configure the drive again.

❑ **ERROR ENCOUNTERED INITIALIZING HARD DRIVE**

When you can't initialize the hard drive, ensure the following things:

1. The adapter is installed correctly
2. All cables are correctly and firmly attached
3. The correct hard drive type is selected in BIOS Setup

❑ **ERROR INITIALIZING HARD DISK CONTROLLER**

When this error occurs, ensure the following things:

1. The cord is exactly installed in the bus.
2. The correct hard drive type is selected in BIOS Setup
3. Whether all of the jumpers are set correctly in the hard drive

❑ **FLOPPY DISK CONTROLLER ERROR OR NO CONTROLLER PRESENT**

When you cannot find or initialize the floppy drive controller, please ensure the controller is in proper BIOS Setup. If there is no floppy drive installed, ensure the Diskette Drive selection in Setup is set to NONE.

❑ **KEYBOARD ERROR OR NO KEYBOARD PRESENT**

When this situation happens, please check keyboard attachment and no keys being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in BIOS Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot procedure.

❑ **MEMORY ADDRESS ERROR**

When the memory address indicates error. You can use this location along with the memory map for your system to find and replace the bad memory chips.

❑ **MEMORY SIZE HAS CHANGED**

Memory has been added or removed since last boot. In EISA mode, use Configuration Utility to re-configure the memory configuration. In ISA mode enter BIOS Setup and enter the new memory size in the memory fields.

❑ **MEMORY VERIFYING ERROR**

It indicates an error verifying a value is already written to memory. Use the location along with your system's memory map to locate the bad chip.

❑ **OFFENDING ADDRESS MISSING**

This message is used in connection with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

❑ **REBOOT ERROR**

When this error occurs that requires you to reboot. Press any key and the system will reboot.

❑ **SYSTEM HALTED**

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Technical Reference

Real-Time Clock and Non-Volatile RAM

The FB2642 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte

Address	Description
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

CMOS RAM Map

Register	Description
00h -10h	Standard AT-compatible RTC and Status and Status Register data definitions
11h – 13h	Varies
14h	<p>Equipment</p> <p>Bits 7-6 Number of Floppy Drives</p> <p>00 1 Drive</p> <p>01 2 Drives</p> <p>Bits 5-4 Monitor Type</p> <p>00 Not CGA or MDA 01 40x25 CGA</p> <p>01 2 Drives 80x25 CGA</p> <p>Bits 3 Display Enabled</p> <p>0 Disabled</p> <p>1 Enabled</p> <p>Bit 2 Keyboard Enabled</p> <p>00 Not CGA or MDA 01 40x25 CGA</p> <p>01 2 Drives 80x25 CGA</p> <p>Bit 1 Math Coprocessor Installed</p> <p>0 Absent</p> <p>1 Present</p> <p>Bit 0 Floppy Drive Installed</p> <p>0 Disabled</p> <p>1 Enabled</p>
15h	Base Memory (in 1KB increments), Low Byte
16h	Base Memory (in 1KB increments), High Byte
17h	IBM-compatible memory (in 1KB increments), Low Byte
18h	IBM-compatible memory (in 1KB increments), High Byte (max 15 MB)
19h-2Dh	Varies
2Eh	Standard CMOS RAM checksum, high byte
2Fh	Standard CMOS RAM checksum, low byte
30h	IBM-compatible Extended Memory, Low Byte (POST) in KB
31h	IBM-compatible Extended Memory, High Byte (POST) in KB
32h	Century Byte
33h	Reserved. Do not use
34h	Reserved. Do not use
35h	Low byte of extended memory (POST) in 64 KB
36h	High byte of extended memory (POST) in 64 KB
37h-3Dh	Varies
3Eh	Extended CMOS Checksum, Low Byte (including 34h-3Dh)
3Fh	Extended CMOS Checksum, High Byte (including 34h-3Dh)

I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. There is a total of 1K-port address space available. The following table lists the I/O port addresses used on the Industrial CPU Card.

Address	Device Description
000h - 00Fh	DMA Controller #1
020h - 021h	Interrupt Controller #1
040h - 043h	Timer
060h - 064h	Keyboard Controller
070h - 071h	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0A1h	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278 - 27F	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)
540h-54Eh	SMBUS Controller
C000h-CFFFh	PCI-PCI Bridge
DF00h-DFEEh	USB Controller
FF00h-FF0Eh	IDE Controller

Interrupt Request Lines (IRQ)

There are a total of 15 IRQ lines available on the Industrial CPU Card. Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on the Industrial CPU Card.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Ethernet
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	SMBus
IRQ11	USB
IRQ12	PS2 Mouse
IRQ13	Math coprocessor
IRQ14	Primary IDE
IRQ15	Secondary IDE

DMA Channel Map

The equivalent of two 8237A DMA controllers are implemented in the FB2650 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Serial Ports

The ACEs (Asynchronous Communication Elements ACE1 to ACE2) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

❑ **Receiver Buffer Register (RBR)**

Bit 0-7: Received data byte (Read Only)

❑ **Transmitter Holding Register (THR)**

Bit 0-7: Transmitter holding data byte (Write Only)

❑ **Interrupt Enable Register (IER)**

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Interrupt Identification Register (IIR)**

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

□ **MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Line Status Register (LSR)**

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

□ **MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

□ **Divisor Latch (LS, MS)**

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Parallel Ports

❑ **Register Address**

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

❑ **Printer Interface Logic**

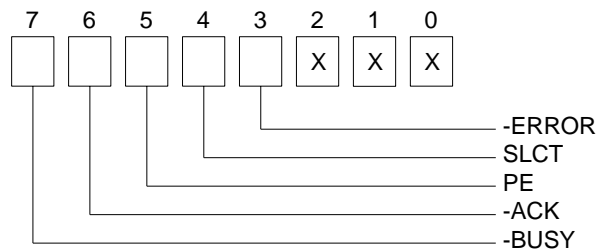
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

❑ **Data Swapper**

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address

❑ **Printer Status Buffer**

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

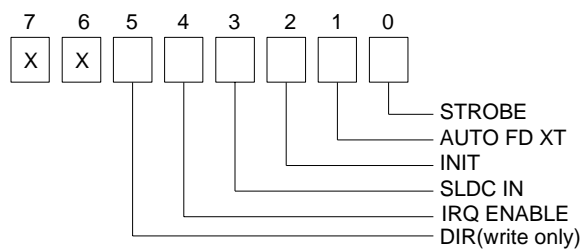


NOTE: X represents not used.

- Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.
- Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.
- Bit 5: A 1 means the printer has detected the end of the paper.
- Bit 4: A 1 means the printer is selected.
- Bit 3: A 0 means the printer has encountered an error condition.

□ **Printer Control Latch & Printer Control Swapper**

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

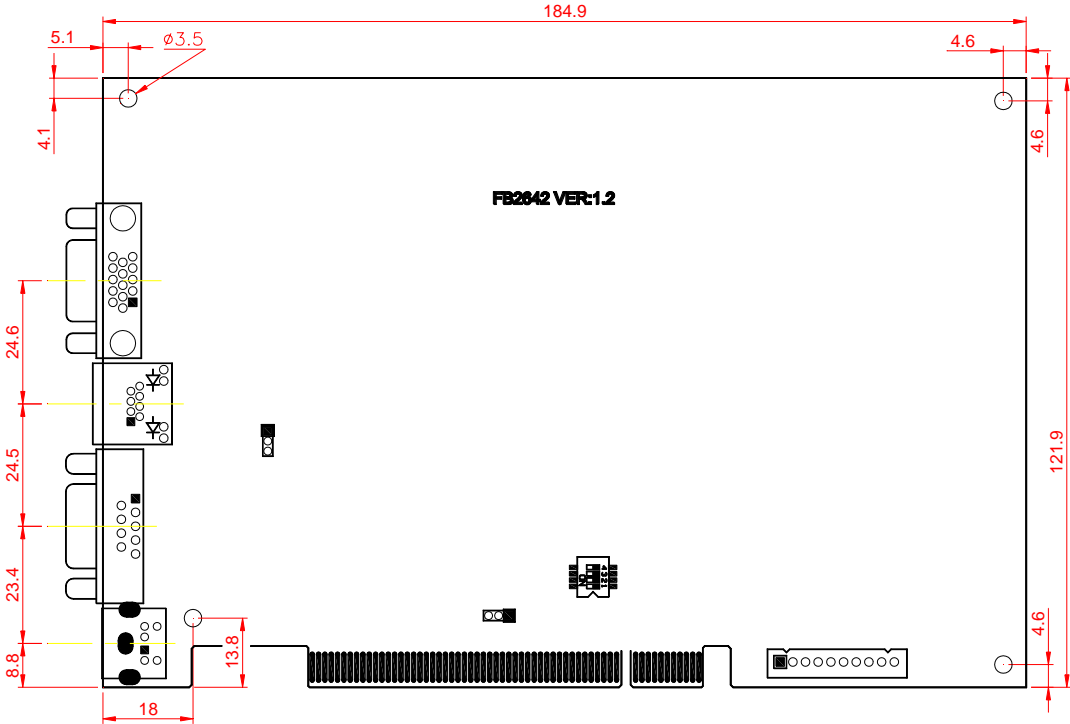


NOTE: X represents not used.

- Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write-only.
- Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.
- Bit 3: A 1 in this bit position selects the printer.
- Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).
- Bit 1: A 1 causes the printer to line-feed after a line is printed.
- Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

Appendix

Dimension



Unit: mm

