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IPC Solution

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FB6500 NS Geode Low Power CPU board User's Manual

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- ❑ A list of your name, address, telephone, facsimile number, or email address where you may be reached during the day
- ❑ Description of you peripheral attachments
- ❑ Description of your software (operating system, version, application software, etc.) and BIOS configuration
- ❑ Description of the symptoms (Extract wording any message)

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Chapter 1 Introducing the FB6500 System Board

Overview

The FB6500 is an all-in-one, compact size, NS Geode low power CPU board. This user's manual provides information on the physical features, installation, and BIOS setup of the FB6500.

Built to unleash the total potential of the Pentium Processor, the FB6500 is all-in-one CPU boards computer capable of handling today's demanding requirements. Able to support 200-300 MHz CPUs, this system board supports 10/100M interface network port, synchronous pipe line burst SDRAM 32/64MB, and a 4MB PCI-VGA controller that can support both LCD's and CRT's simultaneously or independently.

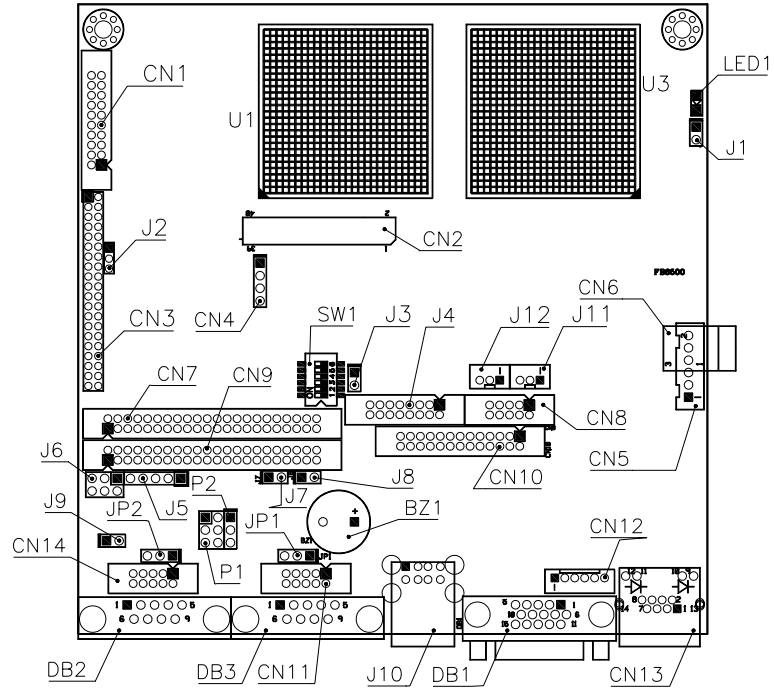
Each FB6500 has four ports for I/O communications. One RS-232C/485 and three RS-232C ports are available.

The FB6500 is perfect for POS and POI applications, network systems, panel / MMI's, order entry kiosks, test equipment, OEM projects or as a motherboard for a panel PC. The unit is only 127X127mm, offering unparalleled performance in a very small footprint.

Series Comparison Table

Model	FB-6500	FB-6500A	FB-6500B
Processor	GX1-300Mhz	GX1-200Mhz	GX1-300Mhz
Chipset	CS5530A	CS5530A	CS5530A
BIOS	AWARD	AWARD	AWARD
Max. SDRAM	64MB	32MB	64MB
VGA CRT/LCD	CS5530A	CS5530A	CS5530A
LVDS	(OPTION)	(OPTION)	(OPTION)
Watchdog Timer	Yes	Yes	Yes
Multi I/O Chip	4S1P	2S1P	2S1P
Enhanced IDE	Yes	Yes	Yes
USB	Yes	Yes	Yes
IrDA	Yes	Yes	Yes
Audio	Yes	No	No
FB4612B	Yes	No	No
Ethernet (10/100Mbps)	One	One	One
Board Size	127mm x 127mm	127mm x 127mm	127mm x 127mm

Layout



Specifications

- ❑ Supports 200~300 MHz NS Geode GX1 CPU.
- ❑ NS CS5530 (A) chipset with UMA architecture.
- ❑ 32MB SDRAM onboard or 64 MB SDRAM onboard (Option).
- ❑ 100M/10M Ethernet with RJ-45 connector.
- ❑ Provides CRT, LCD, and LCD-LVDS interface with 1.5MB to 4MB shared memory.
- ❑ 1 parallel port and 1 PCI IDE Interface.
- ❑ 3 RS-232C and 1 RS-232C/RS-485 with infrared and touch screen interface.
- ❑ PS/2 compatible keyboard and mouse interface.
- ❑ On-board buzzer and LED indicator.
- ❑ Software programmable watchdog timer.
- ❑ On-board Audio.
- ❑ 2 USB ports and TTL I/Os (2 inputs and 2 outputs,).
- ❑ Single +5V/2.5A maximum (Without LCD panel and LCD inverter).
- ❑ EMI Considered on every output signals.
- ❑ Compact size, 127 mm x 127 mm. (5.0" x 5.0").

Packing List

Upon receiving the package, verify the following things. Should any of the mentioned happens, contact us for immediate service.

- Unpack and inspect the FB6500 package for possible damage that may occur during the delivery process.
- Verify the accessories in the package according to the packing list and see if there is anything missing or incorrect package is included.
- If the cable(s) you use to install the FB6500 is not supplied from us, please make sure the specification of the cable(s) is compatible with the FB6500 system board.

Note: after you install the FB6500 series, it is recommended that you keep the diskette or CD that contains drivers and document files, and keep the document copies, or unused cables in the carton for future use.

The following lists the accessories that may be included in your FB6500 package. Some accessories are optional items that are only shipped upon order.

- One FB6500 all-in-one CPU board.
- One 44-pin hard disk driver interface cable.
- One 20-pin to 34-pin floppy disk interface cable.
- One parallel port interface cable.
- Two serial port adapter cables. (10-pin IDC to DB-9, 4-serial-port version only)
- One keyboard and mouse port adapter
- One audio adapter with FB4612B transfers board (Audio version only).
- One power adapter cable.
- One compact disk includes software utility.

Chapter 2 Hardware Installation

To set up a FB6500 system board, complete the description in Chapter 2 and Chapter 3.

This chapter introduces the system board connectors & jumper settings, and guides you to apply them for field application.

Before Installation

Before you install the system board, make sure you follow the following descriptions.

1. Before removing the board from its anti-static bag, wear an anti-static strap to prevent the generation of Electricity Static Discharge (ESD). The ESD may be created from human body that touches the board. It may do damage to the board circuit.
2. Install or unplug any connector, module, or add-on card, be sure that the power is disconnected from the system board. If not, this may damage the system board components, module, or the add-on-card.
3. Installing a heat sink is necessary for heat dissipation from your CPU. If heat sink is not mounted, this may cause the CPU fail due to over-heating problem.

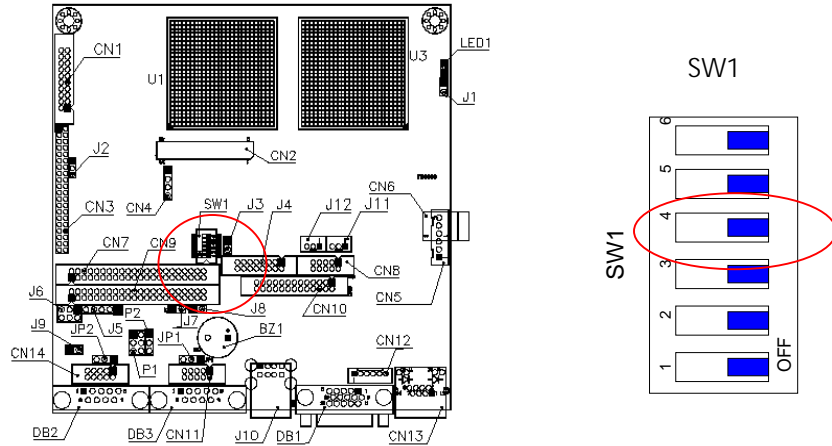
Hardware Features

Index to Connectors/Jumpers/Others

The following lists the connectors and jumpers to install the FB6500.

Item	Description
(SW1-1, SW1-2, & SW1-3)	CPU Internal clock multiplier select
SW1-4	CPU base clock select
CN1	Floppy connector
CN2	18-bit LCD interface connector
CN3	Extension bus connector
CN4	Control signals and power source for LCD inverter.
CN5	2.0mm power connector
CN7	Reserved
CN9	IDE hard disk connectors
CN8	10-pin audio connector
CN10	Parallel port connector
CN11, CN14	Two RS232C Connector
CN12	6-pin 2.0mm keyboard and mouse connector
CN13	LAN connector
DB1	CRT connector
DB2, DB3	One RS232C/RS485 and One RS232C DB9 Connector
J1	Power LED header
J2	Flash BIOS write protect jumper
J3	Reset header
J4	16-pin LVDS-LCD interface connector for long distant LCD panel connection.
J5, J11, J12	Extra RS-232C and infrared connector (10-pin 2.0mm IDC)
J6	TTL I/O connector (option)
J7	HDD LED header
J8	External speaker header
J9	RS-485 mode terminator on and off
P1/P2	RS-485 mode jumper select for serial port 3

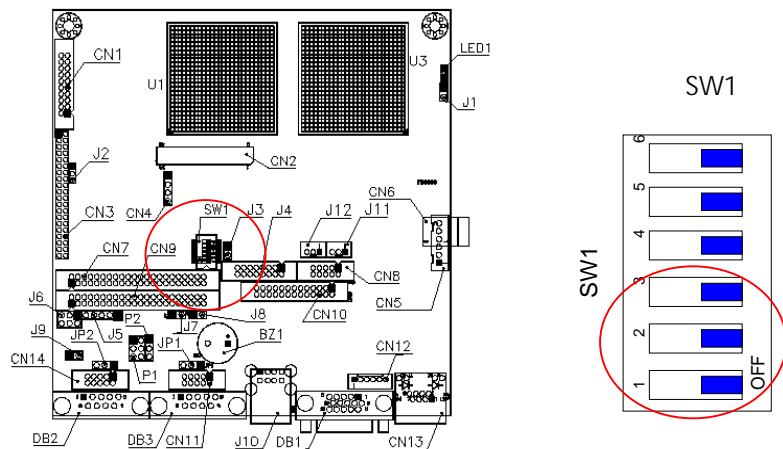
SW1-4: Selecting the CPU Base Clock and PCI Clock



The following table lists the switch settings of the CPU Base Clock and PCI clock.

SW1-4	CPU Base Clock	PCI Clock	Remark
On	30.0 MHz	30.0 MHz	
Off	33.3 MHz	33.3 MHz	Default

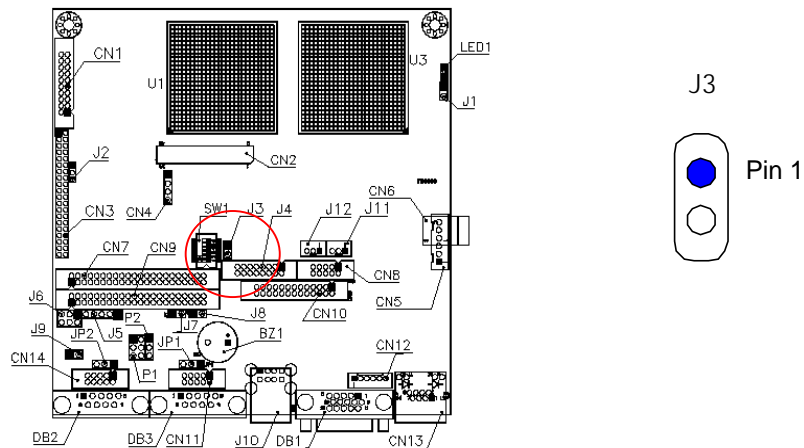
SW1-1, SW1-2, SW1-3: Selecting the CPU Internal Clock Multiplier



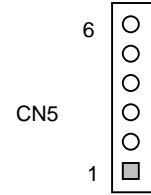
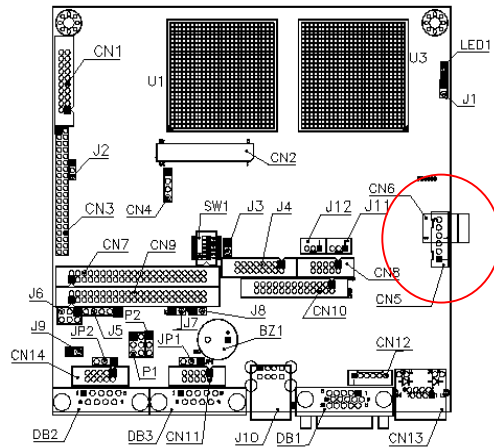
SW1-3	SW1-2	SW1-1	Multiplier	Remark
On	On	On	Reserved	
Off	On	On	10.0	
On	Off	On	9.0	300Mhz Presetting
Off	Off	On	5.0	
On	On	Off	4.0	
Off	On	Off	6.0	200MHz, Default
On	Off	Off	7.0	266MHz Presetting
Off	Off	Off	8.0	233Mhz Presetting

J3: Reset Header

J3 is a 2-pin header for connecting to system reset bottom. Short-circuit these 2 pins to hardware reset FB6500 as well as restart system. It is similar to power off the system and then power it on again.

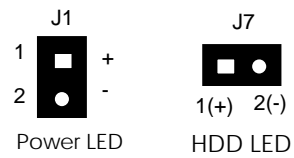
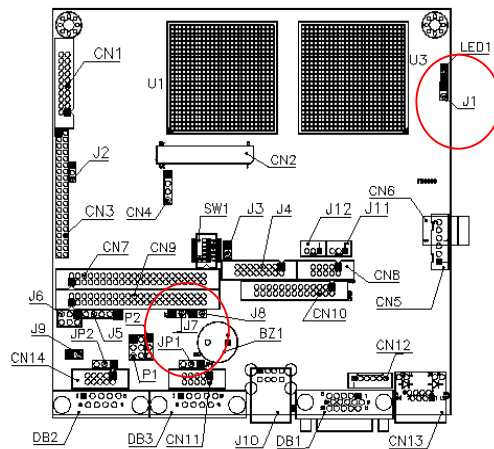


CN5: 6-pin Power Connector (Standard P8 & P9)



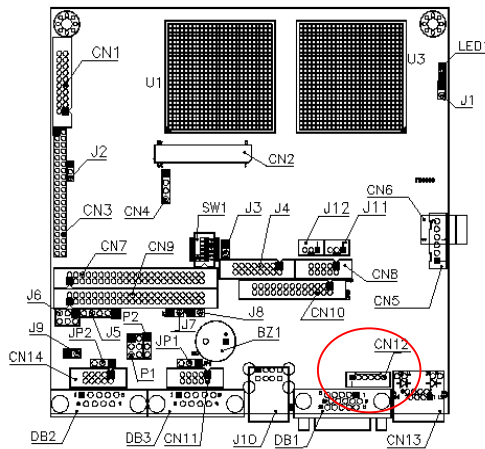
- Pin 1: Ground
 - Pin 2: VCC (+5V)
 - Pin 3: VCC (+5V)
 - Pin 4: Ground
 - Pin 5: Ground
 - Pin 6: + 12V
- Note: If LCD function does not in use, +12V is no need.

J1: Power LED & J7: HDD LED



CN12 Keyboard/Mouse Connector

CN12 is a 6-pin 2.0mm JST connector, use the included adapter cable you can attach standard PS/2 type keyboard and mouse.



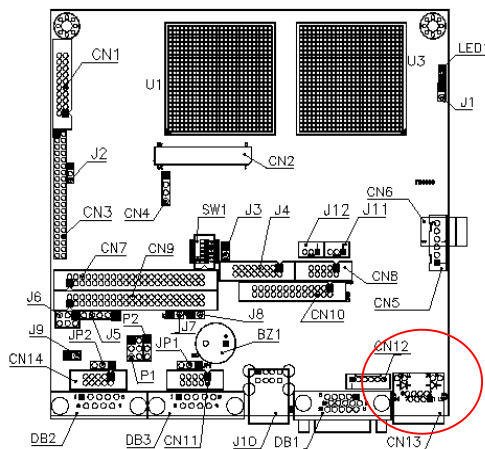
CN12



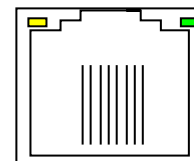
- Pin 1: Ground
- Pin 2: VCC (+5V)
- Pin 3: Keyboard Data
- Pin 4: Keyboard Clock
- Pin 5: Mouse Data
- Pin 6: Mouse Clock

CN13: RJ45 LAN Connector with LED indicators

CN13 is a RJ45 connector with 2 LEDs. The upper right LED (orange) indicates data is being accessed and the upper left LED (green) indicates on-line status. (On indicates on-line and off indicates off-line) The following table lists the pin assignments of CN13.



CN13

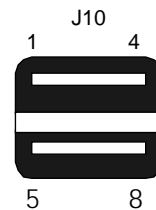
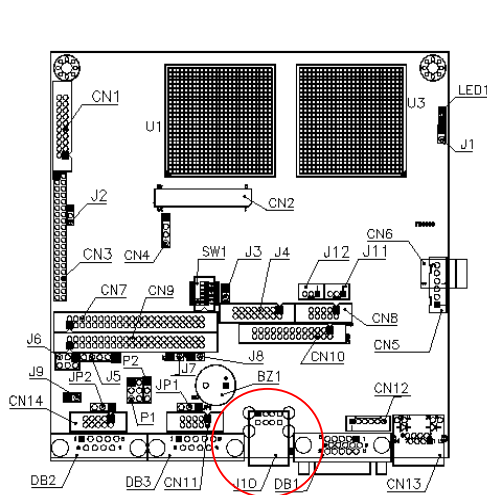


The following lists the pin assignment of CN13.

CN13	Signal	CN13	Signal
1	TPTX+	5	FBG1
2	TPTX -	6	TPRX -
3	TPRX+	7	FBG2
4	FBG1	8	FBG2

J10: USB Connector

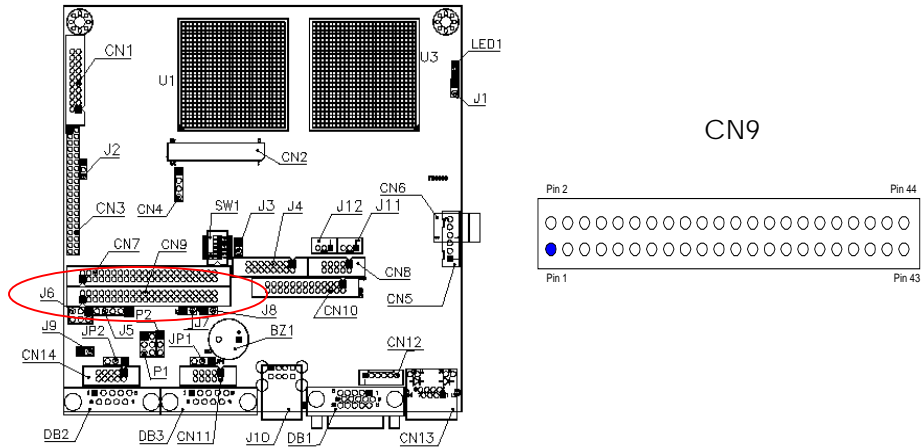
J10 is a dual port USB connector. Any USB device can be attached to J10 with plug-and-play supported. The up side port of J2 is USB #1 and the down side port is USB #2.



- Pin 1: USBV0 Pin5: USBV1
- Pin 2: USBD0- Pin6: USBD1-
- Pin 3: USBD0+ Pin7: USBD1+
- Pin 4: USBG0 Pin8: USBG1
- Pin 9,10: Case Ground Pin11,12: Case Ground

CN9: IDE hard Disk Connectors

CN9 is 44-pin 2.0mm IDC connectors. Use the included hard disk cables to attach up to two 2.5" hard disk drives.

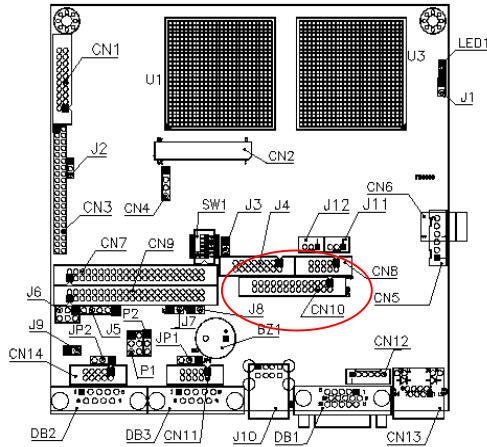


The following table lists the pin description of CN9.

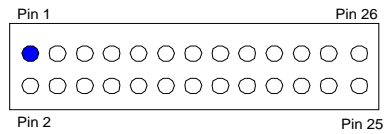
Pin	Description	Pin	Description
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIRDYA	28	GROUND
29	-DACKA	30	GROUND
31	AINT	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41	VCC	42	VCC
43	GROUND	44	Not Used

CN10: 26-pin Parallel Port Connector

The included printer interface cable is used to transfer 26-pin connector into standard DB25 connector.



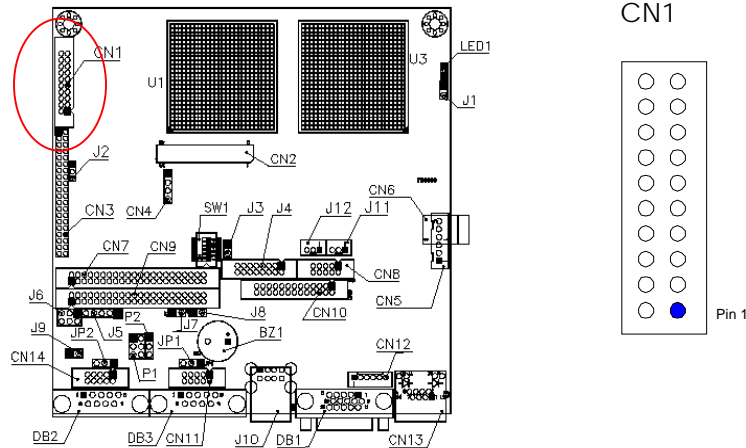
CN10: Parallel Port Connector



CN10	DB-25	Description	CN10	DB-25	Description
1	1	-STROBE	2	14	-AUTO FORM FEED
3	2	DATA 0	4	15	-ERROR
5	3	DATA 1	6	16	-INITIALIZE
7	4	DATA 2	8	17	-PRINTER SELECT IN
9	5	DATA 3	10	18	Ground
11	6	DATA 4	12	19	Ground
13	7	DATA 5	14	20	Ground
15	8	DATA 6	16	21	Ground
17	9	DATA 7	18	22	Ground
19	10	-ACKNOWLEDGE	20	23	Ground
21	11	BUSY	22	24	Ground
23	12	PAPER	24	25	Ground
25	13	PRINTER SELECT	26	--	No Used

CN1: 20-pin Floppy Connector

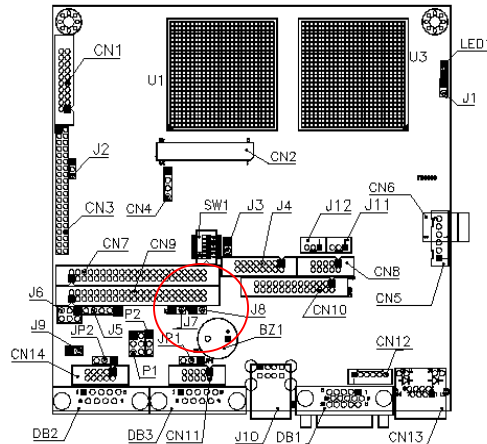
The included floppy drive interface cable is used to transfer 20-pin connector into standard 34-pin connector. The following table shows signal connections between 20-pin & 34-pin connectors.



The following table shows signal connections between 20-pin & 34-pin connectors.

CN1	Description	34-pin	CN1	Description	34-pin
1	Drive Enable A	2	11	-Write Data	22
2	-Index	8	12	Ground	23
3	-Select A	12	13	-Write Enable	24
4	Ground	11	14	-Track 0	26
5	-Motor A	16	15	-Write Protect	28
6	- Select B	14	16	Ground	29
7	-Motor B	10	17	-Read Data	30
8	Ground	9	18	-Head	32
9	-Direction	18	19	-Disk Change	34
10	-Step	20	20	Ground	31
-	-	-	-	No Connection	Others

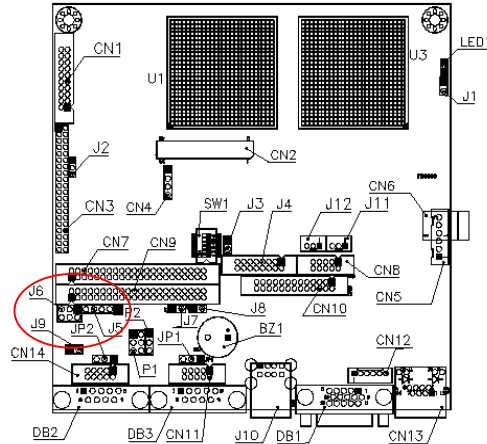
J8: External Speaker Header



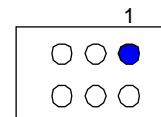
Pin 1: Speaker+
Pin 2: Speaker-

Note: This header is optional

J6: 6-pin TTL I/O Connector (optional)



J6: TTL I/O connector

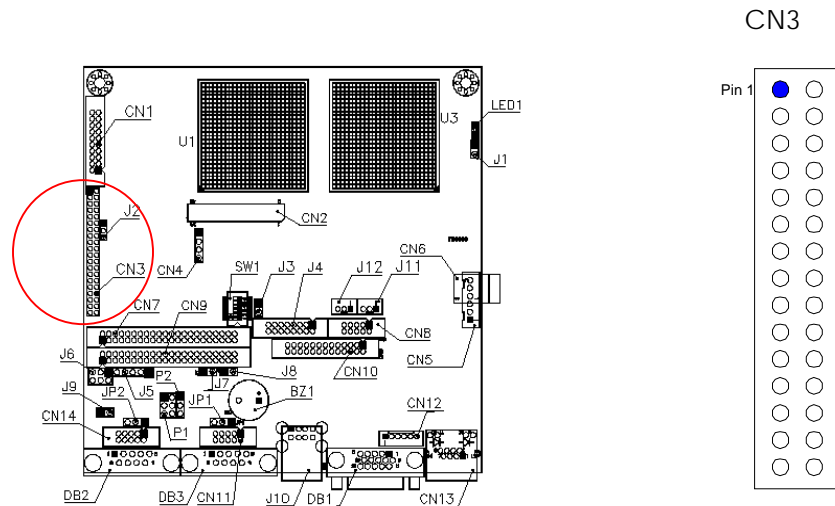


J6	Description	Bit Location	J6	Description	Bit Location
1	Output 0	BIT 0 of I/O port 390H	2	Input 0	BIT 3 of I/O port 390H
3	Output 1	BIT 0 of I/O port 390H	4	Input 1	BIT 4 of I/O port 390H
5	+5V	-	6	Ground	-

Note 1: The I/O address of 390h and reserved memory segment is CC00:0 to CFFF:0.

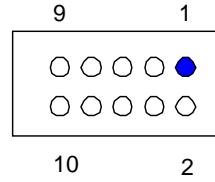
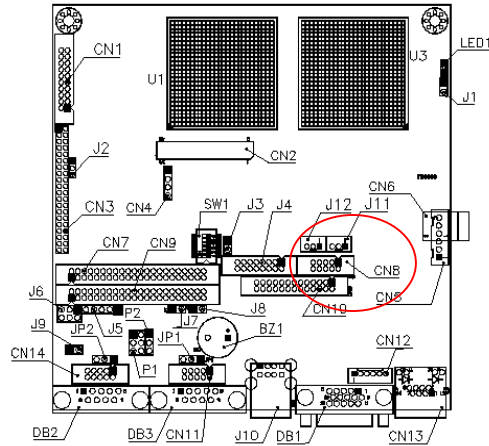
CN3: Extension Bus Connector (optional)

The CN3 connector supports a little signals of ISA for easy debugging or testing. It is reserved for board manufacture only.



CN3	Description	CN3	Description
1	SD7	2	Ground
3	SD6	4	RSTDRV
5	SD5	6	-IOW
7	SD4	8	-IOR
9	SD3	10	ISACLK
11	SD2	12	+5V
13	SD1	14	Not Used
15	SD0	16	SA7
17	AEN	18	SA6
19	+5V	20	SA5
21	SA11	22	SA4
23	SA10	24	SA3
25	SA9	26	SA2
27	SA8	28	SA1
29	Ground	30	SA0

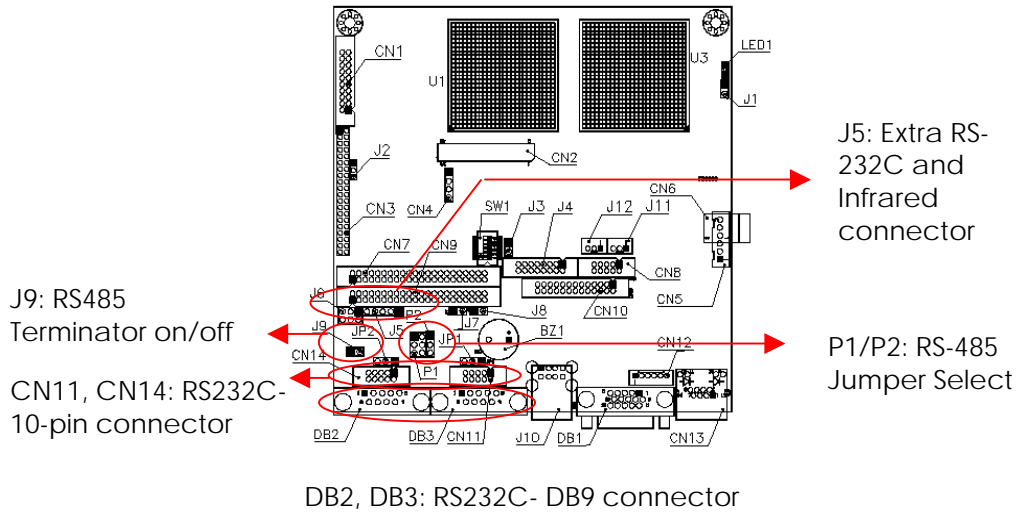
CN8: 10-Pin Audio Connector (optional)



CN8	Description	CN8	Description
1	CDINL	2	LININL
3	CDINR	4	LININR
5	VCC	6	ANALOG GND
7	LINOUTL	8	MICIN
9	LINOUTR	10	GND

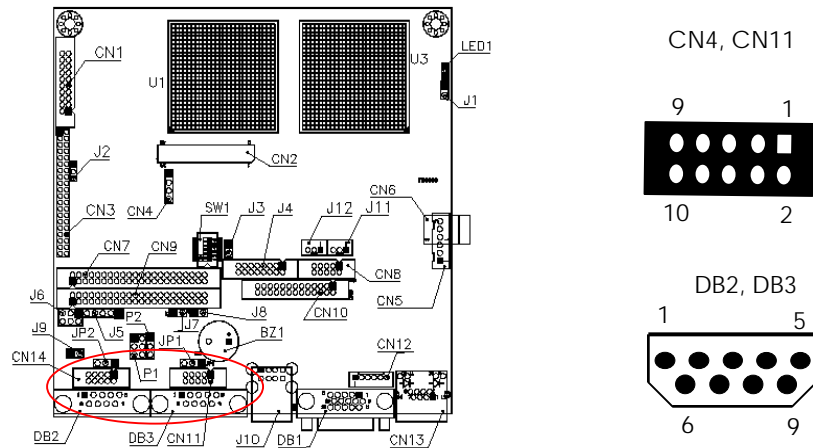
Serial Port Connectors and Jumper Settings

The following figure shows the serial port connector positions and settings.



□ **RS-232C Pin Definitions (DB2, DB3, CN11, and CN14)**

DB3 (COM1) and DB2 (COM2) are all standard serial port connectors; CN11 (COM3) and CN14 (COM4) are both 10-pin 2.0mm IDC connectors. The included serial port adapter cables are used to transfer 10-pin 2.0mm IDC into standard DB-9 connector. The following tables show the signal connections of these connectors and the included adapter cable for CN11 and CN14:

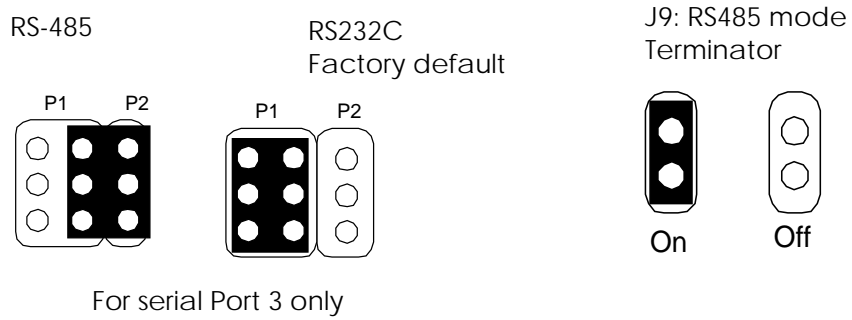


DB3	Signal (COM1)	DB2	Signal (COM2)	RS-485 (COM2)
1	-DCD1	1	-DCD2	-
6	-DSR1	6	-DSR2	-
2	RXD1	2	RXD2	485-
7	-RTS1	7	-RTS2	-
3	-TXD1	3	-TXD2	485+
8	-CTS1	8	-CTS2	-
4	-DTR1	4	-DTR2	-
9	-RI1	9	-RI2	-
5	GROUND	5	GROUND	-

CN11	Signal (COM3)	DB9	CN14	Signal (COM4)	DB9
1	-DCD3	1	1	-DCD4	1
2	-DSR3	6	2	-DSR4	6
3	RXD3	2	3	RXD4	2
4	-RTS3	7	4	-RTS4	7
5	-TXD3	3	5	-TXD4	3
6	-CTS3	8	6	-CTS4	8
7	-DTR3	4	7	-DTR4	4
8	-RI3	9	8	-RI4	9
9	GROUND	5	9	GROUND	5
10	GROUND	Shield	10	GROUND	Shield

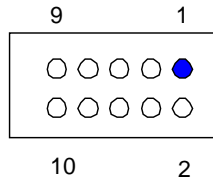
□ **P1/P2: RS-485 Jumper Select and Pin Definitions & J9: RS485 Terminator on/off**

Serial port 1 provides RS-485 function by selecting P1/P2 jumper. When RS-485 mode is selected, the RS-485 signals use the same connector as RS-232C. J9 is the terminator on/off jumper only when using RS-485 mode. The following figure and table guide you how to setup RS-485 serial port.



□ **J5: Extra RS-232C and Infrared Connector (10-pin 2.0mm IDC)**

J5 provides basic RS-232C signals of serial port 3 and infrared signals of serial port 4. The RS-232C signal of serial port 3 is used to interface with touch screen controller internally and infrared signal is used to interface with Infrared modules. If an I.R. device is installed, also enter the BIOS> Peripheral Setup, select an I.R protocol from the Serial Port D Mode field.



J5	Description	J5	Description
1	Not Used	2	VCC
3	RXD3	4	Not Used
5	TXD3	6	IRRX
7	Ground	8	Ground
9	Not Used	10	IRTX

Chapter 3 Installing CRT and LCD Monitors

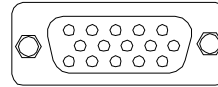
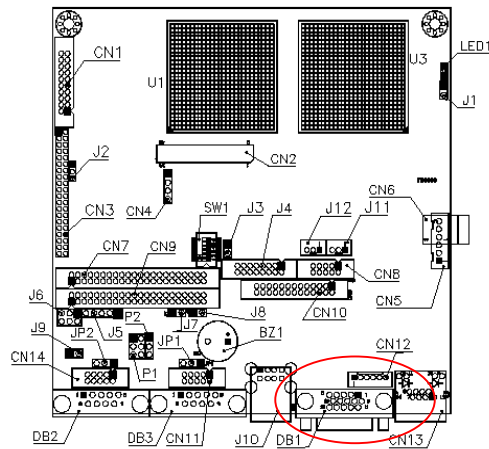
This chapter describes the configuration and installation procedure of LCD and CRT displays. Both CRT and LCD displays may be used at the same time. Only TFT type LCDs may be used. CRT monitors should work with no problem under Windows 95/98. However, each type of LCD requires different BIOS.

The FB6500 supports a CRT colored monitor and a TFT LCD (DSTN LCDs are not supported with this board). It can be connected to create a compact video solution for the industrial environment. 4MB of RAM on-boarded allows a maximum CRT resolution of 1024X768 with 64k colors and a LCD resolution of 800X600 with 64k colors. Different VGA display modes are possible, but your monitor must possess certain characteristics (different modes require different drivers to display the mode desired).

- LCD Flat Panel Display
- CRT & LCD Display

CRT Display (DB1)

A VGA connector is provided for CRT display.

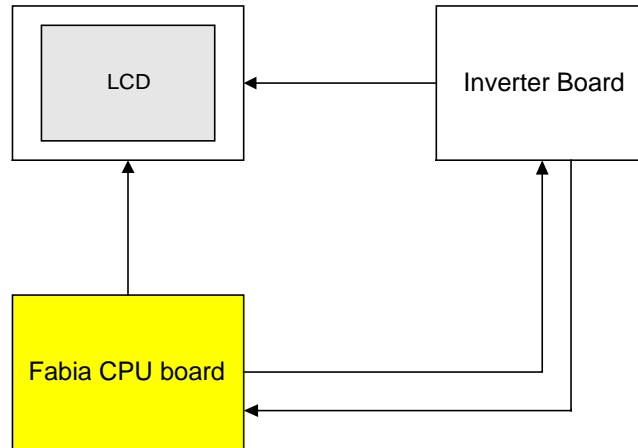


- Pin 1: Red
- Pin 2: Green
- Pin 3: Blue
- Pin 13: Hsync
- Pin 14: Vsync
- Pin 12: DDC Data
- Pin 15: DDC Clock
- Pin 5 & 10: Digital Ground
- Pin 6,7,8: Analog Ground
- Others: Not Used

LCD FLAT PANEL DISPLAY

Each LCD model requires specific BIOS in order to work properly. If you want to use a panel that your board was not originally designed for then, please send an email to support@fabiatech.com and state the LCD type and full specification you use.

The following shows the block diagram of using FB6500 for LCD display.



LCD Panel Block Diagram

The block diagram shows that FB6500 still needs components to be used with a LCD panel. It needs control for the brightness and the contrast of the LCD panel while inverter board is the one that supplies the high voltage to drive the LCD panel.

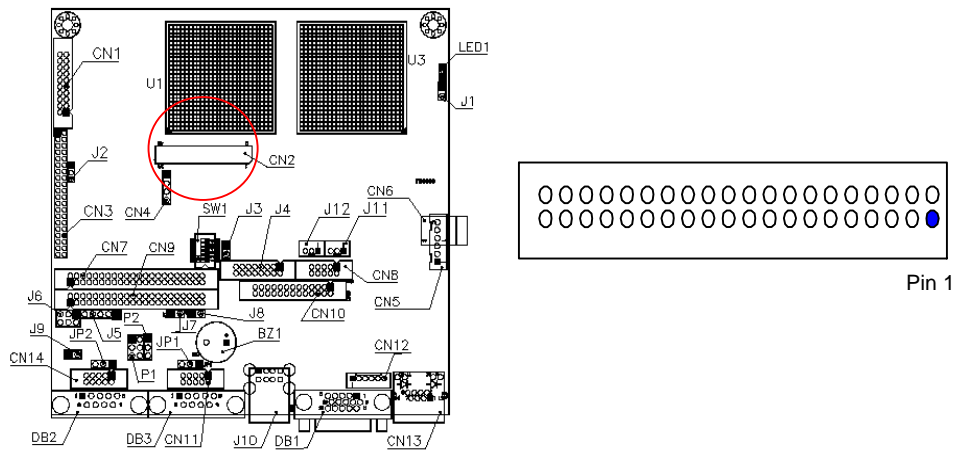
NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable usually has a different color.

CN2: LCD Connector

CN2 is an 18-bit LCD interface connector. The pin assignments are listed in the following table.

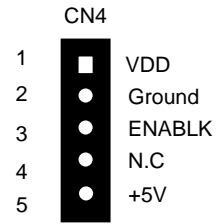
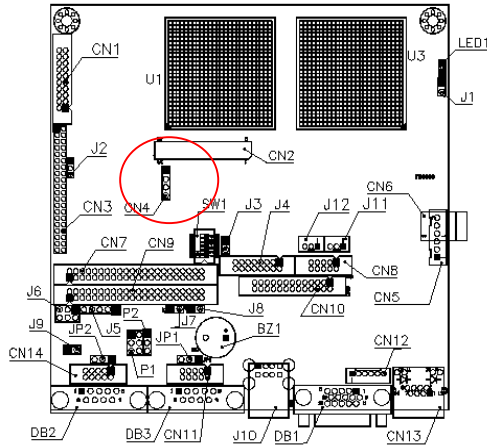
CN2	Description	CN2	Description	CN2	Description	CN2	Description
1	+5V	21	FPD8	2	+5V	22	FPD9
3	Ground	23	FPD10	4	Ground	24	FPD11
5	+ 3.3V	25	N.C	6	+ 3.3V	26	N.C
7	R/L	27	FPD12	8	Ground	28	FPD13
9	N.C	29	FPD14	10	N.C	30	FPD15
11	FPD0	31	FPD16	12	FPD1	32	FPD17
13	FPD2	33	Ground	14	FPD3	34	Ground
15	FPD4	35	FPCLK	16	FPD5	36	FPVSYNC
17	N.C	37	FPDISP	18	N.C	38	FPHSYNC
19	FPD6	39	U/D	20	FPD7	40	FPVDDEN

Note: N.C. means not connected, it is reserved for upgraded signals.



CN4: Control Signals and Power Source for LCD inverter.

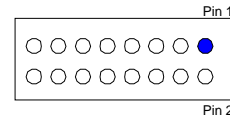
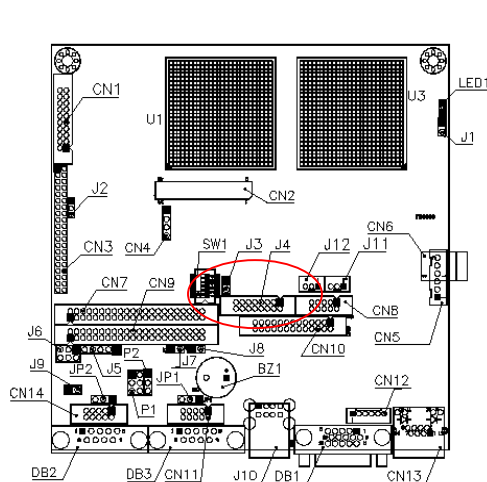
CN4 provides control signals and power source for LCD inverter.



Note: VDD (+12V) is come from CN9 (power connector) only

J4: LVDS-LCD interface connector

J4 is a 16-pin LVDS-LCD interface connector for long distant LCD panel connection.



J4	Description	J4	Description
1	+3.3V	2	+3.3V
3	Ground	4	Ground
5	LVDS0+	6	LVDS0-
7	LVDS1+	8	LVDS1-
9	LVDS2+	10	LVDS2-
11	LVDSCLK+	12	LVDSCLK-
13	Ground	14	Ground
15	FPBKLEN	16	VDD

Note: VDD comes from CN5 (power connector) only.

Chapter 4 BIOS Setup

This chapter describes the BIOS setup.

Overview

BIOS are a program located on a Flash memory chip on a circuit board. It is used to initialize and set up the I/O peripherals and interface cards of the system, which includes time, date, hard disk drive, the ISA bus and connected devices such as the video display, diskette drive, and the keyboard. This program will not be lost when you turn off the system.

The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

All the changes you make will be saved in the system RAM and will not be lost after power-off.

When you start the system, the BIOS will perform a self-diagnostics test called Power On Self Test (POST) for all the attached devices, accessories, and the system. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

Note: Change the parameters when you fully understand their functions and subsequence.

```
ROM PCI/ISA BIOS (2A434FJ9)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP      INTEGRATED PERIPHERALS
BIOS FEATURES SETUP      SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP   USER PASSWORD
POWER MANAGEMENT SETUP   IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION    SAVE & EXIT SETUP
LOAD BIOS DEFAULTS       EXIT WITHOUT SAVING
LOAD SETUP DEFAULTS

Esc : Quit                ↑ ↓ → ← : Select Item
F10 : Save & Exit Setup  (Shift)F2 : Change Color
```

BIOS Functions

On the menu, you can perform the following functions

1. Standard CMOS Setup-
2. BIOS Features Setup
3. Chipset Features Setup
4. Advanced Chipset Setup
5. Power Management Setup
6. PNP/PCI Configuration
7. Load BIOS Defaults
8. Load Setup Default
9. Integrated Peripherals Setup
10. User Password
11. IDE Auto Detect
12. Save & Exit Setup
13. Exit Without Saving

Keyboard Convention

On the BIOS, the following keys can be used to operate and manage the menu:

Item	Function
ESC	To exit the current menu or message
Page Up/Page Down	To select a parameter
F10	Save and exit
F2	To change the color of the menu display. F2 is to go forward and F3 is to go backward.
UP/Down Arrow Keys	To go upward or downward to the desired item

Standard CMOS Setup

This section describes basic system hardware configuration, system clock setup and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

```

ROM PCI/ISA BIOS (2A434F19)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Date (mm:dd:yy) : Thu, Aug 23 2001
Time (hh:mm:ss) : 11 : 40 : 22

HARD DISKS          TYPE      SIZE  CYLS HEAD PRECOMP  LANDZ SECTOR  MODE
-----
Primary Master    :    0    0    0    0    0    0    0    CHS
Primary Slave     :    0    0    0    0    0    0    0    CHS
Secondary Master  :    0    0    0    0    0    0    0    CHS
Secondary Slave   :    0    0    0    0    0    0    0    CHS

Drive A : None
Drive B : None

Video  : EGA/VGA
Halt On : No Errors

ESC : Quit          ↑ ↓ → ← : Select Item      PU/PD/+/- : Modify
F1  : Help          (Shift)F2 : Change Color
    
```

□ Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

□ Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

□ Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

□ **Video**

This option selects the type of adapter used for the primary system monitor that must match your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

You have two ways to boot up the system:

When VGA as primary and monochrome as secondary, the selection of the video type is "VGA Mode".

□ **Error Halt**

This option determines whether the computer will stop if an error is detected during power up.

No errors	The system boot will not be stopped for any error that may be detected.
All errors	Whenever the BIOS detect a non-fatal error the system will be stopped and you will be prompted.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors.
All, But Diskette	The system boot will not stop for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not stop for a keyboard or disk error; it will stop for all other errors.

□ **Memory**

This option is display-only which is determined by POST (Power On Self Test) of the BIOS.

□ **Base Memory**

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memories installed on the motherboard, or 640K for systems with 640K or more memory installed on the motherboard.

□ **Extended Memory**

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

□ **Other Memory**

This refers to the memory located in the 640K to 1024K-address space. This is memory that can be used for different applications. DOS uses this area to load device drivers to keep as much base memory free for application programs. Most use for this area is Shadow RAM.

□ **Total Memory**

System total memory is the sum of basic memory, extended memory, and other memory.

BIOS Features Setup

This section describes the configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

```
ROM PCI/ISA BIOS (2A434FJ9)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.
```

<pre>Virus Warning : Disabled CPU Internal Cache : Enabled Quick Power On Self Test : Enabled Boot Sequence : C,CDROM,A Swap Floppy Drive : Disabled Boot Up Floppy Seek : Enabled Boot Up NumLock Status : On Boot Up System Speed : High Gate A20 Option : Normal Memory Parity Check : Enabled Typematic Rate Setting : Disabled Typematic Rate (Chars/Sec) : 6 Typematic Delay (Msec) : 250 Security Option : Setup PCI/VGA Palette Snoop : Disabled OS Select For DRAM > 64MB : Non-OS2 Report No FDD For WIN 95 : No</pre>	<pre>Video BIOS Shadow : Enabled C8000-CBFFF Shadow : Disabled CC000-CFFFF Shadow : Disabled D0000-D3FFF Shadow : Disabled D4000-D7FFF Shadow : Disabled D8000-DBFFF Shadow : Disabled DC000-DFFFF Shadow : Disabled Cyrix 6x86/MII CPUID : Enabled ESC : Quit ← : Select Item F1 : Help PU/PD/+/- : Modify F5 : Old Values (Shift)F2 : Color F6 : Load BIOS Defaults F7 : Load Setup Defaults</pre>
---	--

Virus Warning

This option may flash on the screen. During and after the system boots up, any attempt to write to the boot sector or partition table of the hard disk drive will halt the system and the following error message will appear, in the mean time, you can run an anti-virus program to locate the problem.

Available Options: Disabled, Enabled

Default setting: Enabled

CPU Internal Cache

This functions speeds up memory access. The FB6500 GXM Cyrix CPU has an internal cache.

Available options: Disabled, Enabled

Default setting: Enabled

Quick Power On Self Test

This option speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enable, BIOS will shorten or skip some items' checks during POST.

□ **Boot Sequence**

This field specifies which device the system looks first upon power on.

Default setting: A, C, SCSI

□ **Swap Floppy Drive**

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of **Disabled** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is **<Enabled>**, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Available options: Disabled, Enabled

Default setting: Disabled

□ **Boot Up Floppy Seek**

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks. 360K types are 40 tracks while 760K, 1.2M and 1.44M are all 80 tracks.

Enabled	BIOS searches for floppy disk drive to determine if it is 40 or 80 tracks. Note that BIOS cannot tell from 720K, 1.2M or 1.44M drive type, as they are all 80 tracks.
Disabled	BIOS will not search for the type of floppy disk drive by track number. Note that there will not be any warning message if the drive installed is 360K.

□ **Gate A20 Option**

This item is chosen as **<Normal>**, the A20 signal is controlled by keyboard controller or chipset hardware. The selection is "Fast" Port 92 or a chipset specific method controls means the A20 signal

Available options: Normal, Fast

Default setting: Normal

□ **BootUp Numlock**

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Available options: On, Off

Default setting: On

Floppy Drive Seek

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.

Available Options: Disabled, Enabled

Default setting: Disabled

Typematic rate Setting

This function specifies the keystroke repeat rate when a key is pressed and held down.

Available options: Fast, Slow

Default setting: Fast

Typematic Rate (Chars/Sec)

Typematic Rate sets the rate at which characters on the screen repeat when a key is pressed and held down.

Available options: 6, 8, 10, 12, 15, 20, 24, or 30 characters per second

Default setting: 6

Typematic Delay (Msec)

The number selected indicates the time period between two identical characters appearing on screen.

Security Option

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Available options: Setup, Always

Default setting: Setup

PCI/VGA Palette Snoop

This option must be set to Enabled if any ISA adapter card installed in the computer requires VGA palette snooping.

Wait for 'F1' If Error

Award BIOS POST error messages are followed by:

Press <F1> to continue

If this field is set to **Disabled**, the Award BIOS does not wait for you to press the <F1> key after an error message.

Available options: Disabled, Enabled

Default setting: Disabled

□ **Hit 'DEL' Message Display**

Set this field to **Disabled** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available options: Disabled, Enabled

Default setting: Enabled

□ **C000, 16k Shadow - DC00, 16k shadow**

These fields control the location of the contents of the 16KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
2. **Enabled:** The contents of C000h - CFFFh are written to the same address in system memory (RAM) for faster execution.
3. **Cached:** The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Available options: Disabled, Enabled, Cached

Default setting: Cached

Chipset FEATURES Setup

This section describes the configuration of the board's chipset features.

```

ROM PCI/ISA BIOS (2A434FJ9)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

SDRAM CAS latency Time : 3 T
SDRAM Clock Ratio Div By : 3

16-bit I/O Recovery (CLK): 5
8-bit I/O Recovery (CLK): 5

USB Controller : Enabled
USB Legacy Support : Disabled

Video Memory Size : 1.5 M
Display status : CRT
Flat Panel Resolution : 640x480

ESC : Quit      ↑↓←→ : Select Item
F1 : Help      PU/PD/+/- : Modify
F5 : Old Values (Shift)F2 : Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults
    
```

□ **SDRAM CAS AUTO Latency Time**

This field specifies the latency for the Synchronous DRAM system memory signals.

Available Options: 3T, 2T

Default setting: 3 T

□ **SDRAM Clock Ration Div by**

When 100 MHz external frequency runs the system, the system will run at 3 cycle clocks. When 66 MHz runs the system, the system will run at 4 cycle clocks. Selecting Auto, the system will be auto adaptive depending on the SDRAM clock that is installed.

Available Options: 4T, 3T

Default setting: 4 T

□ **8bit I/O Recovery Time**

The recovery time is the length of time, measured in CPU clocks, which the system will delay after achieving an input/output request. This delay takes place to wait for the I/O to complete the request. This field specifies the recovery time for 8bit I/O.

Available Options: Disabled, 1 –8 Sysclk

Default setting: 1 Sysclk

16Bit I/O Recovery Time

This field specifies the recovery time for 16Bit I/O.

Available Options: Disabled, 1 –4 Sysclk

Default setting: 1 Sysclk

USB Controller

Select Enabled if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Enabled

Default setting: Enabled

Multiple Monitor Support

This field specifies which VGA display will be used when the system is boot. You can select either the onboard or the VGA card installed on the PCI bus.

Available Options: No Onboard, PCI First, and M/B FIRST

Default setting: Enabled

Video Memory

This field specifies which VGA display memory. You can select either Video memory on the VGA. The setting are share onboard memory.

Available Options: 1.5MB, 2.5MB, and 4MB

Default setting: 2.5MB

Display state

This field specifies which VGA display will be used when the system is boot. You can select either the LCD or the CRT booting on the VGA.

Available Options: Both, LCD, and CRT

Default setting: Both

Flat Panel Resolution

When use the LCD the field specifies which select display resolution for different TFT LCD display type.

Available Options: 640x480, 800x600 and 1024x768

Default setting: 640X480

Power Management

ROM PCI/ISA BIOS (2A434FJ9) POWER MANAGEMENT SETUP AWARD SOFTWARE, INC.			
Power Management	: Disabled	IRQ1 (KeyBoard)	: ON
** PM Timers **		IRQ3 (COM 2)	: OFF
Doze Mode	: Disabled	IRQ4 (COM 1)	: OFF
Standby Mode	: Disabled	IRQ5 (LPT 2)	: OFF
HDD Power Down	: Disabled	IRQ6 (Floppy Disk)	: OFF
MODEM Use IRQ	: NA	IRQ7 (LPT 1)	: OFF
Throttle Duty Cycle	: 33.3 %	IRQ9 (IRQ2 Redir)	: OFF
		IRQ10 (Reserved)	: OFF
		IRQ11 (Reserved)	: OFF
		IRQ12 (PS/2 Mouse)	: OFF
		IRQ13 (Coprocessor)	: OFF
		IRQ14 (Hard Disk)	: OFF
		IRQ15 (Reserved)	: OFF
		ESC : Quit	↑↓←→ : Select Item
		F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift)F2 : Color
		F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

Power Management

The field determines how much power consumption is needed for the system after selecting the below items.

Doze Mode

This field defines the continuous idle time before the system enters Doze Mode.

Standby Mode

This field defines the continuous idle time before the system enters Standby Mode. If any item defined is enabled & active Standby timer will be reloaded.

HDD Power Down

This field specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

Modem Use IRQ

This field specifies the IRQ of the modem.

□ **IRQ-n**

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by BIOS. When any activity occurs, the computer enters Full On mode.

PCI/Plug and Play

ROM PCI/ISA BIOS (2A434F19)
 PNP/PCI CONFIGURATION
 AWARD SOFTWARE, INC.

PNP OS Installed : No Resources Controlled By : Manual Reset Configuration Data : Disabled IRQ-3 assigned to : Legacy ISA IRQ-4 assigned to : Legacy ISA IRQ-5 assigned to : PCI/ISA PnP IRQ-7 assigned to : PCI/ISA PnP IRQ-9 assigned to : PCI/ISA PnP IRQ-10 assigned to : Legacy ISA IRQ-11 assigned to : Legacy ISA IRQ-12 assigned to : PCI/ISA PnP IRQ-14 assigned to : PCI/ISA PnP IRQ-15 assigned to : PCI/ISA PnP DMA-0 assigned to : PCI/ISA PnP DMA-1 assigned to : PCI/ISA PnP DMA-3 assigned to : PCI/ISA PnP DMA-5 assigned to : PCI/ISA PnP DMA-6 assigned to : PCI/ISA PnP DMA-7 assigned to : PCI/ISA PnP	PCI IRQ Activated By : Level Used MEM base addr : N/A ESC : Quit ↑↓←→ : Select Item F1 : Help PU/PD/+/- : Modify F5 : Old Values (Shift)F2 : Color F6 : Load BIOS Defaults F7 : Load Setup Defaults
---	--

- PNP O/S Installed**

Set to Yes to inform BIOS that the operating system can handle Plug and Play (PnP) devices.

Available Options: Yes, No

Default setting: No

- Resources Controlled By:** Auto, Manual

If you select Auto, all the interrupt request (IRQ),DMA assignment, and Used DMA fields disappear, as the BIOS automatically assigns them. The default value is "Manual".

Available Options: Auto, Manual

Default setting: Manual

- Reset Configuration Data:** Enable, Disable

If you select Enable to reset Extended System Configuration Data (ESCD) when you exit setup is you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operation operating system cannot boot.

Available Options: Enable, Disable

Default setting: Disable

□ **IRQ-n/DMA-n Assigned:** PCI/ISA PnP, Legacy ISA

The resources are controlled manually.

1. Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific interrupt/DMA (such as IRQ4, IRQ3 for serial port 1 and 2).
2. PCI/ISA PnP Devices compliant with Plug and play standard, whether designed for PCI or ISA bus.

□ **Use MEM base addr. : Resources Controlled By:** Auto, Manual

Select a base address for the memory area used by any peripheral that requires high memory.

Available Options: N/A, C800, CC00, D000, D400, D800 and DC00

Default setting: N/A

Peripheral Setup

This section describes the function of peripheral features.

ROM PCI/ISA BIOS (2A434FJ9) INTEGRATED PERIPHERALS AWARD SOFTWARE, INC.	
IDE HDD Block Mode	: Disabled
Primary IDE Channel	: Enabled
Master Drive PIO Mode	: Auto
Slave Drive PIO Mode	: Auto
Secondary IDE Channel	: Enabled
Master Drive PIO Mode	: Auto
Slave Drive PIO Mode	: Auto
IDE Primary Master UDMA	: Auto
IDE Primary Slave UDMA	: Auto
IDE Secondary Master UDMA	: Auto
IDE Secondary Slave UDMA	: Auto
Onboard FDC Controller	: Enabled
Onboard Serial Port 1	: 3F8/IRQ4
Onboard Serial Port 2	:
UART Mode Select	:
Onboard Parallel Port	:
Parallel Port Mode	:
ECP Mode Use DMA	: 3
Onboard Serial Port 3	: 3E8
Serial Port 3 Use IRQ	: IRQ11
Onboard Serial Port 4	: 2E8
Serial Port 4 Mode	: Standard
Serial Port 4 Use IRQ	: IRQ10
Build in CPU Audio	: Enabled
Audio I/O Base Address	: 220H
MPU-401 I/O Base Address	: 330H m
Audio IRQ Select	: IRQ 5 y
Audio Low DMA Select	: DMA 1
Audio High DMA Select	: DMA 5
F7	: Load Setup Defaults

IDE HDD Block Mode

This option allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive (HDD).

IDE PIO

IDE hard drive controllers can support up to two separate hard drives. These drives have a master/slave relationship, which is determined by the cabling configuration used to attach them to the controller. Your system supports one IDE controller – a primary and a secondary – so you have the ability to install up to four separate hard disks.

PIO means Programmed Input/Output. Rather than have the BIOS issue a series of commands to affect a transfer to or from the disk drive, PIO allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by them. This is simpler and more efficient (and faster). Your system supports five modes, numbered from 0 to 4, which primarily differ in timing. When Auto is selected, the BIOS will select the best available mode.

OnBoard FDC

This field enables the floppy drive controller on the FB6500.

Available Options: Auto, Disabled, Enabled

Default setting: Auto

OnBoard Serial Port 1

These fields select the I/O port address for each Serial port.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, 3E8H/COM3, 2E8H/COM4

Default setting: 3F8H/COM1

OnBoard Serial Port 2

These fields select the I/O port address for each Serial port.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, 3E8H/COM3, 2E8H/COM4

Default setting: 2F8H/COM2

OnBoard Serial Port 3

These fields select the I/O port address for each Serial port.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, 3E8H/COM3, 2E8H/COM4

Default setting: 3E8H/COM1

OnBoard Serial Port 4

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, 3E8H/COM3, 2E8H/COM4

Default setting: 2E8H/COM4

Serial Port 4 Mode

COM4 can be configured for either IR or normal COM port application. Select Normal when Serial Port B is used to install normal COM port device, or select IrDA or ASK IR for an I.R. device.

Available Options: Normal, IrDA, ASK IR

Default setting: Normal

OnBoard Parallel Port 1

This field selects the I/O port address for parallel port.

Available Options: Auto, Disabled, 378, 278, 3BCH

Default setting: 378H

□ **Parallel Port Mode**

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

Available Options: Normal, Bi-Dir, EPP, and ECP

Default setting: Normal

□ **Parallel Port Use IRQ**

This field specifies the IRQ for the parallel port.

Available Options: 5, 7

Default setting: 7

□ **ECP Mode Use DMA**

This field is read-only and cannot be configured.

Available Options: 0, 1, and 3

Default setting: ECP for DMA3

□ **Build In CPU Audio**

This field specifies the internal Audio Control.

Available Options: Disable, Enable

Default setting: Enable

□ **Audio Base I/O Address**

These fields select the I/O port address for Audio.

Available Options: 220H, 240H, 260H and 280H

Default setting: 220H

□ **Audio IRQ Select**

This field specifies the IRQ for the Audio.

Available Options: Disable, 5,7 and 10

Default setting: 5

□ **Audio Low DMA Select**

This field specifies the DMA for internal Audio Control.

Available Options: Disable, 0, 1 and 3

Default setting: 1

□ **Audio High DMA Select**

This field specifies the DMA for internal Audio Control.

Available Options: Disable, 5, 6 and 7

Default setting: 5

Password Setup

There are two security passwords: Supervisor and User. Supervisor is a privileged person that can change the User password from the BIOS.

According to the default setting, both access passwords are not set up and are only valid after you set the password from the BIOS.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Type the desired password (up to 8 character length) when you see the message, "Enter New Supervisor Password."
3. Then you can go on to set a user password (up to 8 character length) if required. Note that you cannot configure the User password until the Supervisor password is set up.
4. Enter Advanced CMOS Setup screen and point to the Password Checkup field.
5. Select Always or Setup.
 - ✧ **Always:** a visitor who attempts to enter BIOS or operating system will be prompted for password.
 - ✧ **Setup:** a visitor who attempts to the operating system will be prompted for user password. You can enter either User password or Supervisor password.
6. Point to **Save Settings and Exit** and press Enter.
7. Press Y when you see the message, "Save Current Settings and Exit (Y/N)?"

Note: it is suggested that you write down the password in a safe place to avoid that password may be forgotten or missing.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Press Enter instead of entering any character when you see the message, "Enter New Supervisor Password."
3. Thus you can disable the password.

Chapter 5 Driver and Utility

The enclosed diskette includes FB6500 VGA, AUDIO driver a LAN driver.

VGA Drivers

WIN98/WIN95 Driver

- 1 To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>FB6500>VGA>WIN98. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.
- 2 Execute CYRIXM-1.exe file.
- 3 The screen shows the SETUP type. Press any key to enter the main menu.
- 4 As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

LAN Utility & Driver

- 1 To install the LAN utility OR driver, insert the CD ROM into the CD ROM device, and enter DRIVER>FB6500>LAN. If your system is not equipped with a CD ROM device, copy the LAN VGA driver from the CD ROM to a 1.44" diskette.
- 2 Execute install.exe file.

Note: In the LAN directory, a HELPME.EXE file is included to provide installation information

Audio Drivers

WIN 95/98 Driver

- 1 To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>FB6500>AUDIO>WIN98. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.
- 2 Execute CYRIM~1.EXE file.
- 3 The screen shows the SETUP type. Press any key to enter the main menu.
- 4 As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

Programming RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 precedes the transmission, which needs control the TXC signal, and the installing, steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

Note: Please refer to the section of the "Serial Ports" in the Chapter "System Controllers" for the detail description of the COM port's register.

□ **Initialize COM port**

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the FB6500 CPU card's DTR signal to the RS-485' s TXC communication.

□ **Send out one character (Transmit)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

□ **Send out one block data (Transmit – the data more than two characters)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

□ **Receive data**

The RS-485's operation of receiving data is in the same of the RS-232's.

□ **Basic Language Example**

a. Initial 86C450 UART

```
10 OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20 REM Reset DTR
30 OUT &H3FC, (INP(%H3FC) AND &HFA)
40 RETURN
```

b. Send out one character to COM1

```
10 REM Enable transmitter by setting DTR ON
20 OUT &H3FC, (INP(&H3FC) OR &H01)
30 REM Send out one character
40 PRINT #1, OUTCHR$
50 REM Check transmitter holding register and shift register
60 IF ((INP(&H3FD) AND &H60) >0) THEN 60
70 REM Disable transmitter by resetting DTR
80 OUT &H3FC, (INP(&H3FC) AND &HEF)
90 RETURN
```

□ **c. Receive one character from COM1**

```
10 REM Check COM1: receiver buffer
20 IF LOF(1)<256 THEN 70
30 REM Receiver buffer is empty
40 INPSTR$
50 RETURN
60 REM Read one character from COM1: buffer
```

70 INPSTR\$=INPUT\$(1,#1)

80 RETURN

NOTE: The example of the above program is based on COM1 (I/O Address 3F8h).
The RS-485 of the FB6500 uses COM2. If you want to program it, please
refer to the BIOS Setup for COM3 address setup.

Chapter 6 Error Coding

This section outlines the errors that may occur when you operate the system, and also gives you the suggestions on solving the problems.

Topic include:

- Trouble Shooting for Error Messages
- Trouble Shooting for POST Code

Trouble Shooting for Error Messages

The following information informs the error messages and troubleshooting. Please adjust your systems according to the messages below. Make sure all the components and connectors are in proper position and firmly attached. If the errors still exist, please contact with your distributor for maintenance.

□ **POST BEEP**

Currently there are two kinds of beep codes in BIOS setup.

- One indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by three short beeps.
- The other indicates that an error has occurred in your DRAM. This beep code consists of a constant single long beep.

□ **CMOS BATTERY FAILURE**

When the CMOS battery is out of work or has run out, the user has to replace it with a new battery.

❑ **CMOS CHECKSUM ERROR**

This error informs that the CMOS has corrupted. When the battery runs weak, this situation might happen. Please check the battery and change a new one when necessary.

❑ **DISPLAY SWITCH IS SET INCORRECTLY**

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in BIOS Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter BIOS Setup and change the video selection.

❑ **DISK BOOT FAILURE**

When you can't find the boot device, insert a system disk into Drive A and press < Enter >. Make sure both the controller and cables are all in proper positions, and also make sure the disk is formatted. Then reboot the system.

❑ **DISKETTE DRIVES OR TYPES MISMATCH ERROR**

When the diskette drive type is different from CMOS, please run setup or configure the drive again.

❑ **ERROR ENCOUNTERED INITIALIZING HARD DRIVE**

When you can't initialize the hard drive, ensure the following things:

1. The adapter is installed correctly
2. All cables are correctly and firmly attached
3. The correct hard drive type is selected in BIOS Setup

❑ **ERROR INITIALIZING HARD DISK CONTROLLER**

When this error occurs, ensure the following things:

1. The cord is exactly installed in the bus.
2. The correct hard drive type is selected in BIOS Setup
3. Whether all of the jumpers are set correctly in the hard drive

❑ **FLOPPY DISK CONTROLLER ERROR OR NO CONTROLLER PRESENT**

When you cannot find or initialize the floppy drive controller, please ensure the controller is in proper BIOS Setup. If there is no floppy drive installed, ensure the Diskette Drive selection in Setup is set to NONE.

❑ **KEYBOARD ERROR OR NO KEYBOARD PRESENT**

When this situation happens, please check keyboard attachment and no keys being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in BIOS Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot procedure.

❑ **MEMORY ADDRESS ERROR**

When the memory address indicates error. You can use this location along with the memory map for your system to find and replace the bad memory chips.

❑ **MEMORY SIZE HAS CHANGED**

Memory has been added or removed since last boot. In EISA mode, use Configuration Utility to re-configure the memory configuration. In ISA mode enter BIOS Setup and enter the new memory size in the memory fields.

❑ **MEMORY VERIFYING ERROR**

It indicates an error verifying a value is already written to memory. Use the location along with your system's memory map to locate the bad chip.

❑ **OFFENDING ADDRESS MISSING**

This message is used in connection with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

❑ **REBOOT ERROR**

When this error occurs that requires you to reboot. Press any key and the system will reboot.

❑ **SYSTEM HALTED**

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Trouble Shooting for Post Codes

When you power on your PC, and the screen display nothing. You have to insert the POST Card for test. The address for ISA POST port is 80h. Make sure the card is in correct slot. The lists below indicate you the error messages. Please follow the instruction to adjust your system. If the error still occurred, please contact with your distributor for maintenance.

- **C0: Turn off OEM specific cache, shadow...**
- **03: Initialize all the standard devices with default values Standard devices includes:**
 1. DMA controller (8237).
 2. Programmable Interrupt Controller (8259).
 3. Programmable Interval Timer (8254).
 4. RTC chip.
- **05:**
 1. Keyboard Controller Self-Test.
 2. Enable Keyboard Interface.
- **07: Verifies CMOS's basic R/W functionality.**
- **BE: Program defaults values into chipset according to the Combinable Chipset Default Table.**
- **C1: Auto-detection of onboard DRAM & Cache.**
- **C5: Copy the BIOS from ROM into E0000-FFFF shadow RAM so that POST will go faster.**
- **08: Test the first 256K DRAM.**
- **09:**
 1. Program the configuration register of Cyrix CPU according to the Combinable Cyrix Register Table.
 2. OEM specific cache initialization (if needed).

- **0A:**
 1. Initialize the first 32-interrupt vectors with corresponding Interrupt handlers
Initialize INT no from 33-120 with Dummy (Spurious) Interrupt Handler.
 2. Issue CUID instruction to identify CPU type.
 3. Early Power Management initialization (OEM specific).

- **0B:**
 1. Verify the RTC time is valid or not.
 2. Detect bad battery.
 3. Read CMOS data into BIOS stack area.
 4. PnP initializations including (PnP BIOS only).
 - Assign CSN to PnP ISA card.
 - Create resource map from ESCD.
 5. Assign I/O & Memory for PCI devices (PCI BIOS only).

- **0C: Initialization of the BIOS Data Area (40: 0N-40:FF).**

- **0D:**
 1. Program some of the Chipset's value according to Setup. (Early Setup Value Program).
 2. Measure CPU speed for display & decide the system clock speed.
 3. Video initialization including Monochrome, CGA, EGA/VGA. If no display device is found, the speaker will beep.

- **0E:**
 1. Initialize the APIC (Multi-Processor BIOS only).
 2. Test video RAM (If Monochrome display device found).
 3. Show messages including
 - Award Logo, Copyright string, BIOS Date code & Part No.
 - OEM specific sign on messages.

-Energy Star Loge (Green BIOS only).

-CPU brand, type & speed.

-Test system BIOS checksum (Non-compress Version only).

- **0F: DMA channel 0 test.**
- **10: DMA channel 1 test.**
- **11: DMA page registers test.**
- **14: Test 8254 Timer 0 Counter2.**
- **15: Test 8259 interrupts mask bits for channel 1.**
- **16: Test 8259 interrupts mask bits for channel 2.**
- **19: Test 8259 functionality.**
- **30: Detect Base Memory & Extended Memory Size.**
- **31**
 1. Test Base Memory from 256K to 640K.
 2. Test Extended Memory from 1M to the top of memory.
- **32:**
 1. Display the Award Plug & Play BIOS Extension message (PnP BIOS only).
 2. Program all onboard super I/O chips (if any) including COM ports, LPT ports, and FDD port.... according to setup value.
- **3C: Set flag to allow users to enter CMOS Setup Utility.**
- **3D:**
 1. Initialize Keyboard.
 2. Install PS2 mouse.
- **3E: Try to turn on Level 2 cache.**

Note: Some chipset may need to turn on the L2 cache in this stage. But usually, the cache is turn on later in POST 61h.

- **3F:**
 1. Program the rest of the Chipset's value according to Setup. (Later Setup Value Program).
 2. If auto-configuration is enabled, programmed the chipset with pre-defined value in the Combinable Auto-Table.
- **41: Initialize floppy disk drive controller.**
- **42: Initialize Hard drive controller.**
- **43: If it is PnP BIOS, initialize serial & parallel ports.**
- **45: Initialize math coprocessor.**
- **4E: If there is any error detected (such as video, kb...), show all the error messages the screen & wait for user to press <F1> key.**
- **4F:**
 1. If password is needed, ask for password.
 2. Clear the Energy Star Logo (Green BIOS only).
- **50: Write all CMOS values currently in the BIOS stack area back into the CMOS.**
- **52:**
 1. Initialize all ISA ROMs.
 2. Later PCI initializations (PCI BIOS only).
 - Assign IRQ to PCI devices.
 - Initialize all PCI ROMs.
 3. PnP Initializations (PnP BIOS only).
 - Assign I/O, Memory, IRQ & DMA TO PnP ISA devices.
 - Initialize all PnP ISA ROMs.
 4. Program shadows RAM according to Setup settings.
 5. Program parity according to Setup setting.
 6. Power Management Initialization.
 - Enable/Disable global PM.

-APM interface initialization.

- **53:**
 1. If it is NOT a PnP BIOS, initialize serial & parallel ports.
 2. Initialize time value in BIOS data area by translate the RTC time value into a timer tick value.

- **60: Setup Virus Protection (Boot Sector Protection) functionality according to Setup setting.**

- **61:**
 1. Try to turn on Level 2 cache.

Note: if L2 cache is already turned on in POST 3D, this part will be skipped.
 2. Set the boot up speed according to Setup setting.
 3. Last chance for Chipset initialization.
 4. Last chance for Power Management initialization (Green BIOS only).
 5. Show the system configuration table.

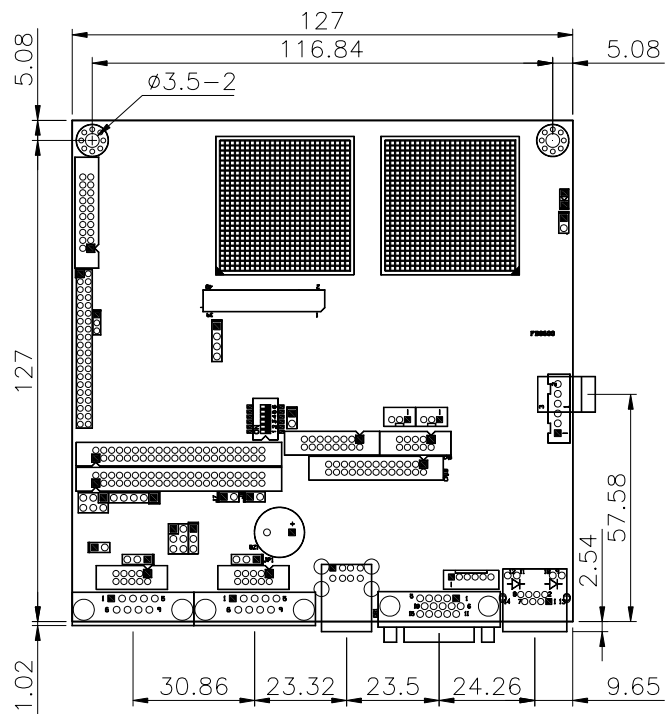
- **62:**
 1. Setup daylight saving according to Setup value.
 2. Program the NumLock, typematic rate & typematic speed according to Setup setting.

- **63:**
 1. If there are any changes in the hardware configuration, update the ESCD information (PnP BIOS only).
 2. Clear memory that has been used.
 3. Boot system via INT 19H.

- **FF: System Booting.** This means that the BIOS already pass the control right to the operating system.

Appendix

Dimension



Technical Reference

Real-Time Clock and Non-Volatile RAM

The FB6500 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte

Address	Description
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

CMOS RAM Map

Register	Description
00h -10h	Standard AT-compatible RTC and Status and Status Register data definitions
11h - 13h	Varies
14h	<p>Equipment</p> <p>Bits 7-6 Number of Floppy Drives</p> <p>00 1 Drive</p> <p>01 2 Drives</p> <p>Bits 5-4 Monitor Type</p> <p>00 Not CGA or MDA 01 40x25 CGA</p> <p>01 2 Drives 80x25 CGA</p> <p>Bits 3 Display Enabled</p> <p>0 Disabled</p> <p>1 Enabled</p> <p>Bit 2 Keyboard Enabled</p> <p>00 Not CGA or MDA 01 40x25 CGA</p> <p>01 2 Drives 80x25 CGA</p> <p>Bit 1 Math Coprocessor Installed</p> <p>0 Absent</p> <p>1 Present</p> <p>Bit 0 Floppy Drive Installed</p> <p>0 Disabled</p> <p>1 Enabled</p>
15h	Base Memory (in 1KB increments), Low Byte
16h	Base Memory (in 1KB increments), High Byte
17h	IBM-compatible memory (in 1KB increments), Low Byte
18h	IBM-compatible memory (in 1KB increments), High Byte (max 15 MB)
19h-2Dh	Varies
2Eh	Standard CMOS RAM checksum, high byte
2Fh	Standard CMOS RAM checksum, low byte
30h	IBM-compatible Extended Memory, Low Byte (POST) in KB
31h	IBM-compatible Extended Memory, High Byte (POST) in KB
32h	Century Byte
33h	Reserved. Do not use
34h	Reserved. Do not use
35h	Low byte of extended memory (POST) in 64 KB
36h	High byte of extended memory (POST) in 64 KB
37h-3Dh	Varies
3Eh	Extended CMOS Checksum, Low Byte (including 34h-3Dh)
3Fh	Extended CMOS Checksum, High Byte (including 34h-3Dh)

I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. There is a total of 1K-port address space available. The following table lists the I/O port addresses used on the Industrial CPU Card.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
390 - 397	TTL I/O
2E8h - 2EFh	Serial Port #4(COM4)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3E8h - 3EFh	Serial Port #3(COM3)
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

Interrupt Request Lines (IRQ)

There are a total of 15 IRQ lines available on the Industrial CPU Card. Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on the Industrial CPU Card.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	AUDIO
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Serial port #3
IRQ10	Reserved
IRQ11	Serial port #4
IRQ12	Reserved
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

DMA Channel Map

The equivalent of two 8237A DMA controllers are implemented in the FB6500 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Serial Ports

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

□ **Receiver Buffer Register (RBR)**

Bit 0-7: Received data byte (Read Only)

□ **Transmitter Holding Register (THR)**

Bit 0-7: Transmitter holding data byte (Write Only)

□ **Interrupt Enable Register (IER)**

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Interrupt Identification Register (IIR)**

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

□ **MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Line Status Register (LSR)**

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

□ **MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

□ **Divisor Latch (LS, MS)**

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Parallel Ports

□ **Register Address**

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

□ **Printer Interface Logic**

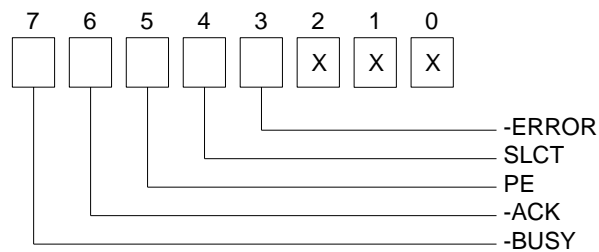
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

□ **Data Swapper**

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address

□ **Printer Status Buffer**

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

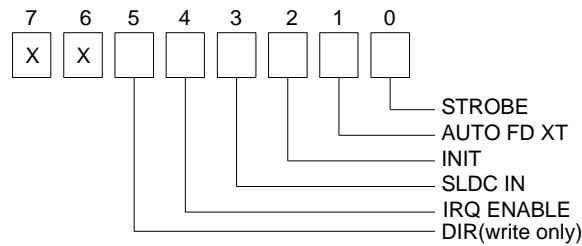


NOTE: X represents not used.

- Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.
- Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.
- Bit 5: A 1 means the printer has detected the end of the paper.
- Bit 4: A 1 means the printer is selected.
- Bit 3: A 0 means the printer has encountered an error condition.

□ **Printer Control Latch & Printer Control Swapper**

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



NOTE: X represents not used.

- Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write-only.

- Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

- Bit 3: A 1 in this bit position selects the printer.

- Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

- Bit 1: A 1 causes the printer to line-feed after a line is printed.

- Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.